

FWA8308 Series

Networking Appliance

User's Manual

Version: 1.0

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Foreword

To prevent damage to the system board, please handle it with care and follow the measures below, which are generally sufficient to protect your equipment from static electricity discharge:

When handling the board, use a grounded wrist strap designed for static discharge elimination grounded to a metal object before removing the board from the antistatic bag. Handle the board by its edges only; do not touch its components, peripheral chips, memory modules or gold contacts.

When handling processor chips or memory modules, avoid touching their pins or gold edge fingers. Return the Network Appliance system board and peripherals back into the antistatic bag when not in use or not installed in the chassis.

Some circuitry on the system board can continue to operate even though the power is switched off. Under no circumstances should the Lithium battery cell used to power the real-time clock be allowed to be shorted. The battery cell may heat up under these conditions and present a burn hazard.

WARNING!

1. "CAUTION: DANGER OF EXPLOSION IF BATTERY IS INCORRECTLY REPLACED.
REPLACE ONLY WITH SAME OR EQUIVALENT TYPE RECOMMENDED BY THE
MANUFACTURER. DISCARD USED BATTERIES ACCORDING TO THE
MANUFACTURER'S INSTRUCTIONS"
2. This guide is for technically qualified personnel who have experience installing and configuring system boards. Disconnect the system board power supply from its power source before you connect/disconnect cables or install/remove any system board components. Failure to do this can result in personnel injury or equipment damage.
3. Avoid short-circuiting the lithium battery; this can cause it to superheat and cause burns if touched.
4. Do not operate the processor without a thermal solution. Damage to the processor can occur in seconds.
5. Do not block air vents at least minimum 1/2-inch clearance required.

FWA8308 series was specifically designed for the network security & management market.

Network Security Applications:

- Firewall
- Unified Threat Management (UTM)
- Virtual Private Network (VPN)
- Proxy Server
- Caching Server

Network Management Applications:

- Load balancing
- Quality of Service
- Remote Access Service

The FWA networking appliance product line covers the spectrum from offering platforms designed for:

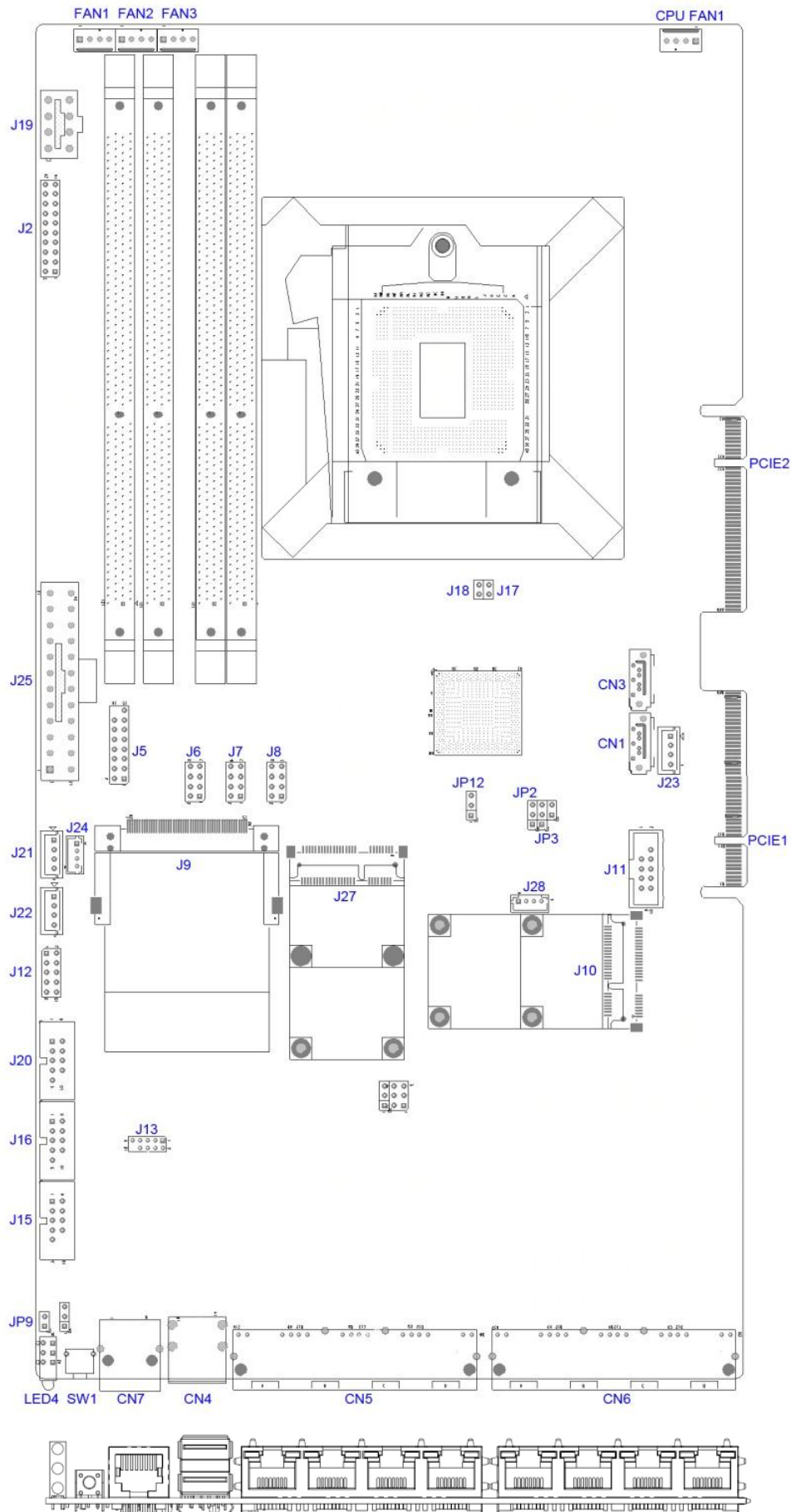
- SOHO
- SMB
- Enterprise

Each product is designed to address the distinctive requirements of its respective market segment from cost effective entry-level solutions to high throughput and performance-bound systems for the Enterprise level.

Product Name	FWA8308																				
Form Factor	19" 1U Mainstream Networking Product																				
Motherboard	MB968																				
Processor	- Support for Intel® Shark Bay DT LGA1150 Haswell processors - TDP = 35W ~ 84W (DC / QC)																				
Chipset	Intel® Lynx Point C226 PCH Package =23 mm x 22 mm , 0.65 mm ball pitch																				
Supported CPUs	- E3-1275 v3 - E3-1225 v3 - E3-1268L v3 - i7-4770TE - i7-4770S - i5-4570S - i5-4570TE - i3-4330 - i3-4330TE - Celeron G1820TE - Celeron G1820 - Pentium G3320TE - Pentium G3420																				
Memory	- Four DDR3 UDIMM total for 32GB max memory (4Gb chip support) - Support DDR3 / DDR3L at 1.5V - Dual channel DDR3 up to 1600 MHz - Unbuffered - ECC or non-ECC																				
Network	- Eth1: Intel® Clarkville I217LM GbE PHY , 6mm x 6mm, QFN48 with iAMT 9.0 supporting. No Bypass - Eth2~4: Intel® Pearsonville I210-AT. No Bypass. - Eth5~6: Intel® Pearsonville I210-AT. Support Bypass. - Eth7~8: Intel® Pearsonville I210-AT. Support Bypass.																				
Expansion Slot	- Two PCI-e x8 Golden Finger - CF Card Socket - Mini PCI-e Socket (m-SATA compatible)																				
Storage	One internal 2.5" HDD (FWA8308 & FWA8308-RPSU) One internal 3.5" HDD (FWA8308-2SLOT)																				
Front Panel	- Two RJ-45 1x4 connectors for Eth1~4 & 5~6 - USB 3.0 x2 - RJ-45 (for console, COM1) - Three LEDs for Power, Bypass & Status - Factory Mode Restore Reset Switch																				
Rear Panel	- PSU inlet 1x or 2x Slot (Depend on product SKU)																				
USB Port	- Two USB 3.0 + 2.0 ports at front panel - One USB 2.0 for Mini PCI-e - Six USB 2.0 pin headers (pitch 2.54) 12 78 <table><tr><th>SignalName</th><th>Pin #</th><th>Pin #</th><th>SignalName</th></tr><tr><td>VCC</td><td>1</td><td>2</td><td>Ground</td></tr><tr><td>USB1-</td><td>3</td><td>4</td><td>USB2+</td></tr><tr><td>USB1+</td><td>5</td><td>6</td><td>USB2-</td></tr><tr><td>Ground</td><td>7</td><td>8</td><td>VCC</td></tr></table>	SignalName	Pin #	Pin #	SignalName	VCC	1	2	Ground	USB1-	3	4	USB2+	USB1+	5	6	USB2-	Ground	7	8	VCC
SignalName	Pin #	Pin #	SignalName																		
VCC	1	2	Ground																		
USB1-	3	4	USB2+																		
USB1+	5	6	USB2-																		
Ground	7	8	VCC																		

ATM	ATM 9.0
TPM	Nuvoton WPCT210AA0WX TPM1.2
VGA	Pin header on board
LCM	2x16 characters LCM
Watchdog Timer	256 segments, 0, 1, 2...255 sec/min
Power Supply	● 300W Single PSU (FWA8308 & FWA8308-2SLOT) ● 275W 1+1 redundant PSU (FWA8308-RPSU)
Dimensions	44 (H) x 440 (W) x 406.5 (D) mm
Operation Temperature	0 ~ 45 ° C
Storage Temperature	-20 ~ 70 ° C
Operation Humidity	5% ~ 95%
Certifications	CE, FCC, LVD
Compatible Front Expansion Cards	● IBP161: 4-port RJ-45 10/100/1000 Copper LAN Module Card ● IBP162: 2-port 10 GbE SFP+ LAN Module Card ● IBP163: 2+2 ports GbE Copper or SFP LAN Module Card ● IBP164: Crypto Acceleration Card ● IBP165: 4-port RJ-45 10/100/1000 Copper LAN Module Card ● IBP167: 8-port RJ-45 10/100/1000 Copper LAN Module Card ● IP331: PCI-e 1-to-1 Riser Card ● IP332: PCI-e Adapter Card (with 2.5" HDD Interface) ● IP333: PCI-e 2-to-2 Riser Card ● IP335: PCI-e 1-to-2 Riser Card

Jumper Locations on MB968



Jumper Settings on MB968

JP2: Clear CMOS Setting

JP2	Setting
	Normal
	Clear CMOS

JP3: Clear ME Setting

JP3	Setting
	Normal
	Clear ME

JP9: AT / ATX Mode Setting

JP9	Setting
	ATX
	AT

JP12: BIOS Flash Security Setting

JP12	Setting
	Normal
	For BIOS Update

JP15: LED Function Selection

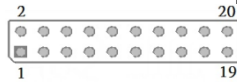
JP15	Setting
	HDD Activate
	Bypass Activate

J17, J18: PCIE Config Setting

J18	J17	Setting
		2 x 8 for Golden Finger PCIE1 & PCIE2
		1x16 for Golden Finger PCIE2

J2: System Function Connector

J2 provides connectors for system indicators that provide light indication of the computer activities and switches to change the computer status. J2 is a 20-pin header that provides interfaces for the following functions



Pin 2, 4, 6, 8: Speaker

This connector provides an interface to a speaker for audio tone generation. An 8-ohm speaker is recommended.

Pin #	Signal Name
2	SPEAKER
4	NC
6	GND
8	+5V

Pin 1, 3, 5: Power LED

The power LED indicates the status of the main power switch.

Pin #	Signal Name
1	+5V
3	NC
5	GND

Pin 13, 14: ATX Power ON Switch

This 2-pin connector is an “ATX Power Supply On/Off Switch” on the system that connects to the power switch on the case. When pressed, the power switch will force the system to power on. When pressed again, it will force the system to power off.

Pin #	Signal Name
13	GND
14	Power_ON

Pin 17, 18: Reset Switch

The reset switch allows the user to reset the system without turning the main power switch off and then on again. Orientation is not required when making a connection to this header.

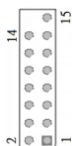
Pin #	Signal Name
17	GND
18	PM_SYSRST#

Pins 19, 20: HDD LED

This connector connects to the hard drive activity LED on control panel. This LED will flash when the HDD is being accessed.

Pin #	Signal Name
19	+3.3V
20	-HDD_LED

J5: VGA Connectors



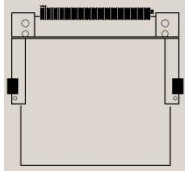
SIGNAL NAME	Pin #	Pin #	Signal Name
VGA_R	1	2	VGA_PWR
VGA_G	3	4	GND
VGA_B	5	6	NC
NC	7	8	VGADDCDATA
GND	9	10	HSYNC
GND	11	12	VSYNC
GND	13	14	VGADDCCLK
GND	15		

J6, J7, J8: USB6~USB11 Ports



SIGNAL NAME	Pin #	Pin #	Signal Name
+5V	1	2	GND
D-	3	4	D+
D+	5	6	D-
GND	7	8	+5V

J9: Compact Flash Socket

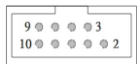


Note: CF card supports IDE mode only.

If CF card applied, please set the SATA configuration to "IDE mode" in BIOS.

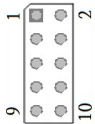
J10: Mini PCI- E / mSATA Socket

J11: SPI Debug Port



SIGNAL NAME	Pin #	Pin #	Signal Name
		2	NC
SPI_CS# 0	3	4	+3.3V
SPI_SO	5	6	SPI0_HOLD#
SPI0_WP#	7	8	SPI_CLK
GND	9	10	SPI_SI

J12: Digital IO 4-IN / 4-OUT Connector



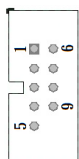
SIGNAL NAME	Pin #	Pin #	Signal Name
GND	1	2	+5V
OUT3	3	4	OUT1
OUT2	5	6	OUT0
IN3	7	8	IN1
IN2	9	10	IN0

J13: LPC Debug Port



Signal Name	Pin #	Pin #	Signal Name
LPC_AD0	1	2	SIO_PLTRST#
LPC_AD1	3	4	LPC_FRAME#
LPC_AD2	5	6	+3.3V
LPC_AD3	7	8	Ground
LPC_CLK	9		

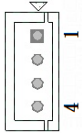
J15, J16, J20: Serial Port (COM1~COM3)



Signal Name	Pin #	Pin #	Signal Name
DCD#	1	6	DSR#
SIN	2	7	RTS#
SOUT	3	8	CTS#
DTR#	4	9	RI#
GND	5		

J19, J25: ATX Power Connector

J21, J22, J23: Power Connector, Pitch 2.54mm



Pin #	Signal Name
1	+5V
2	Ground
3	Ground
4	+12V

J24: Power Connector, Pitch 2.0mm



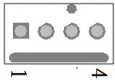
Pin #	Signal Name
1	+5V
2	Ground
3	Ground
4	+12V

J27: mSATA Socket

CN1, CN3: HDD Serial ATA Connector

CPU_FAN1: CPU Fan Connector

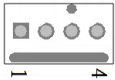
CPU_FAN1 is a 4-pin header for the CPU fan.
The fan must be 12V (Max. 1A).



Pin #	Signal Name
1	Ground
2	+12V
3	Rotation detection
4	Rotation control

FAN1, FAN2, FAN3: System Fan Connectors

FAN1, FAN2, FAN3 is a 4-pin header for system fans.
The fan must be 12V (Max. 1A).



Pin #	Signal Name
1	Ground
2	+12V
3	Rotation detection
4	Rotation control

LED4: Status LED

A1 & C1 : Status LED

A2 & C2 : Bypass or HDD status LED

A3 & C3 : Power LED



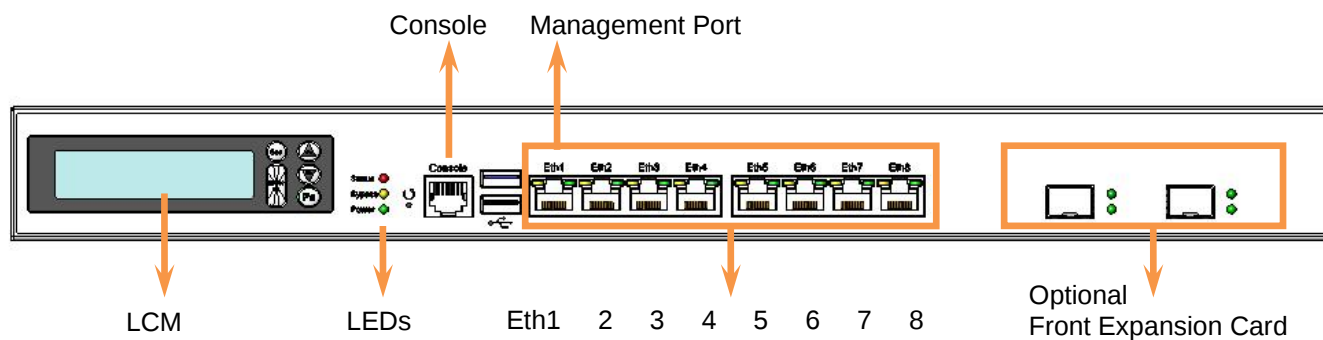
Status

Bypass or HDD

Power

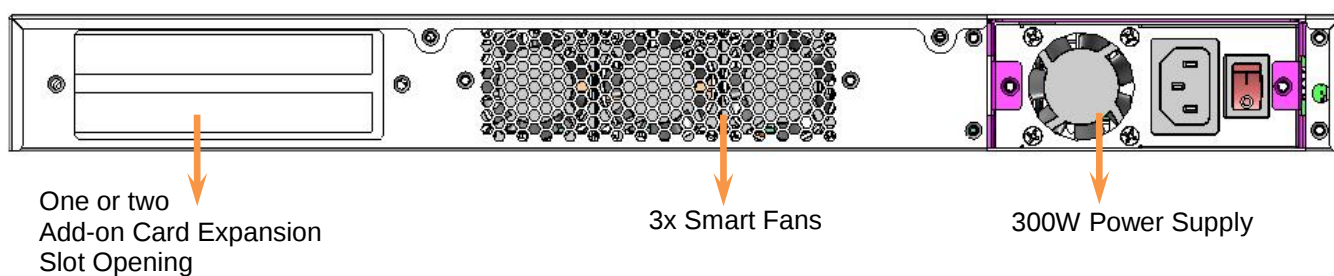
S I G N A L N A M E	Pin #	Pin #	Signal Name
SIO_GPIO33	A1	C1	SIO_GPIO32
+5 V	A2	C2	JP15 Selection
+3.3 V	A3	C3	GND

Front Panel Features

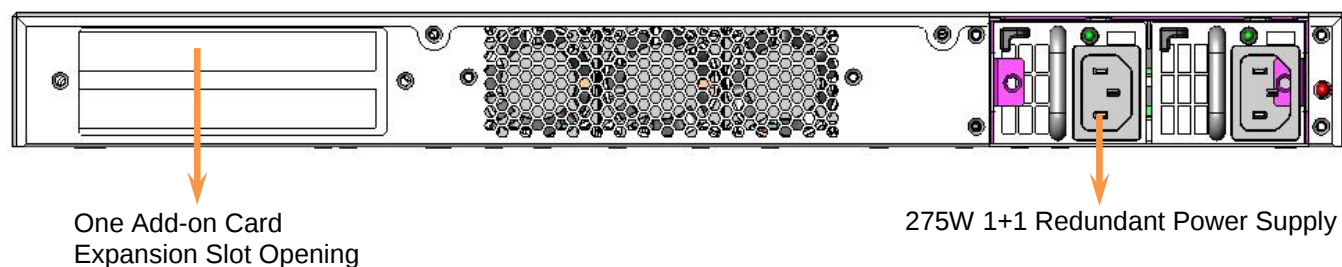


Rear Panel Features

FWA8308 & FWA8308-2SLOT



FWA8308-RPSU



FWA8308 supports output information via Console in BIOS level.

Prepare a computer as client loaded with an existing OS such as Windows XP and Windows 7.
Connect client computer and FWA8308 with NULL Modem cable.

Follow the steps below to configure the Windows Hyper Terminal application setting:

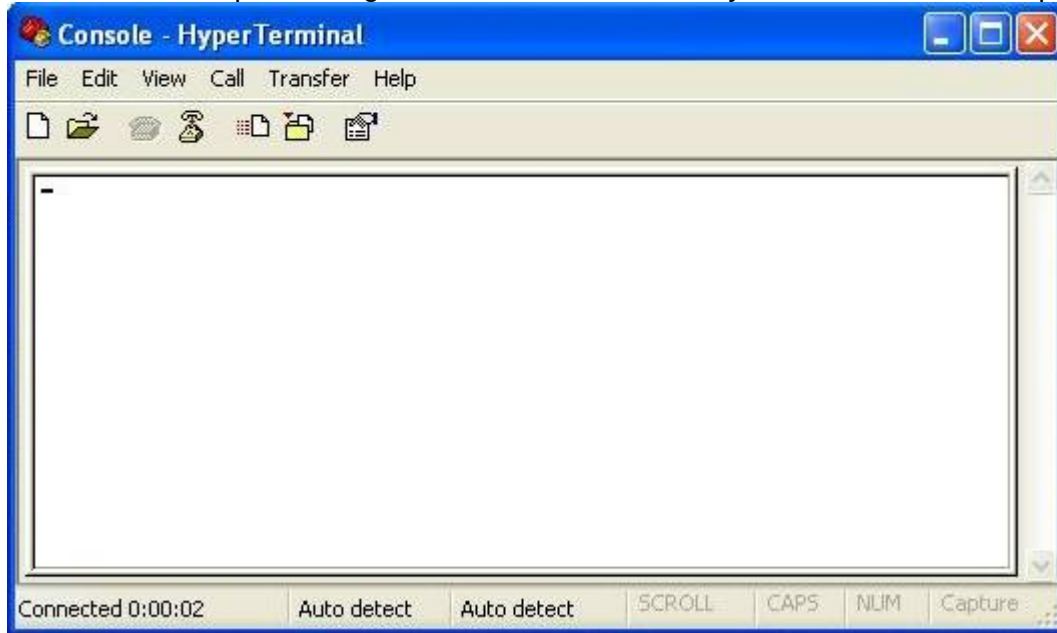
1. Execute Hyper Terminal. Issue command "hypertrm".
2. Customize your name for the new connection.



3. Choose COM port on the client computer for the connection.



4. Please make the port settings to Baud rate 19200, Parity None, Data bits 8, Stop bits 1



5. Power on FWA8308.
Press <Tab> key to enter BIOS setup screen in **Console mode**.
Press key to enter BIOS setup screen in **VGA mode**.

Chapter 5 Open the Chassis

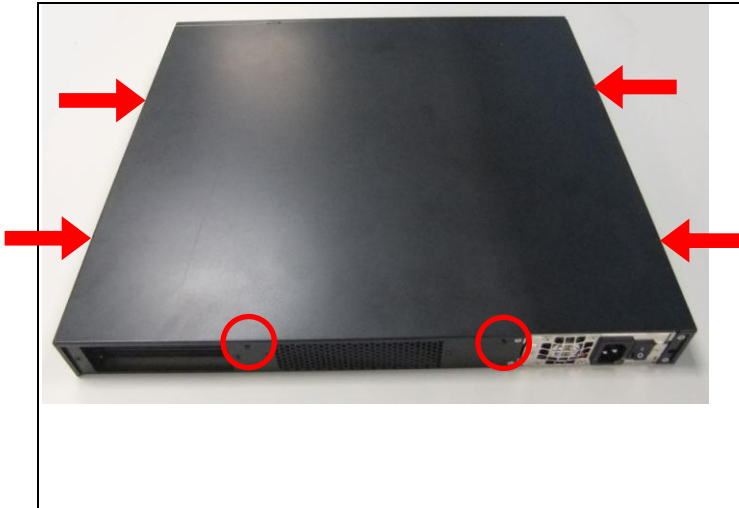


Fig. 5-2 Take off six screws and open the top lead



Fig. 5-3 The base stand

Chapter 6 Installing DDR3 Memory

Install system memory by pulling the socket's arm and pressing it into the slot gently.

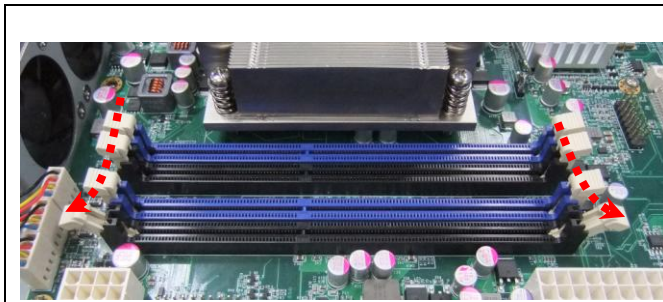


Fig. 6-1 Open both arms on DIMM socket

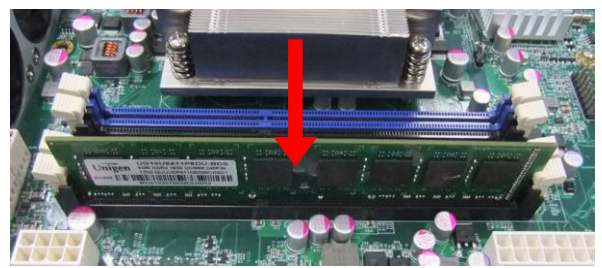


Fig. 6-2 Install DIMM

Notice:

1. MB968 supports two groups of dual channels memory.
One group is on the black DIMM sockets, and the other one is blue DIMM sockets.
2. The recommended height of memory module doesn't exceed 30 mm.

Chapter 7 Installing CompactFlash Card

Insert CompactFlash card into the socket.



Fig. 7-1 Insert CompactFlash Card into the CF interface



Fig. 7-2 Completion of CompactFlash Card connection

Chapter 8 Removing and Installing the Battery

1. Press the metal clip back to eject the button battery.
2. Replace it with a new one by pressing the battery with fingertip to restore the battery

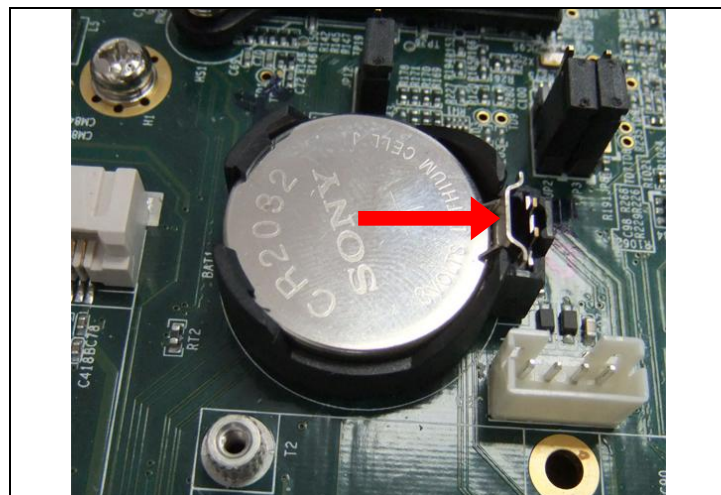


Fig. 8-1 Eject the battery and replace with new one

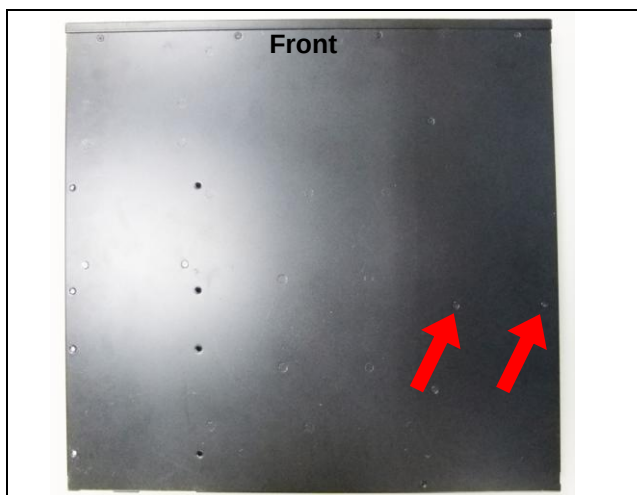


Fig. 9- Take off two screws on bottom to remove 2.5" HDD bracket.



Fig. 9-2 Fasten the four screws to lock HDD and bracket together.



Fig. 9-3 Push HDD into connector



Fig. 9-4 Completion of HDD connection

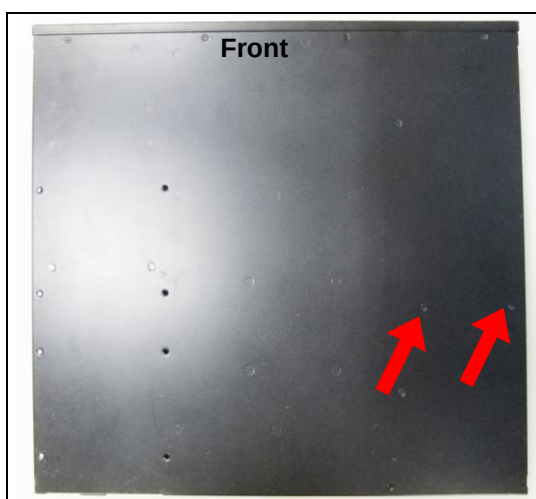


Fig. 9-5 Fix HDD bracket with two screws

Chapter 10 Installing Optional Dual 2.5" HDD Kit

The following is for optional Dual 2.5" HDD kit:

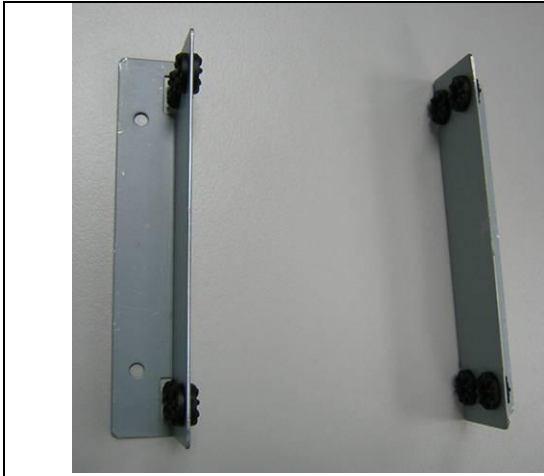


Fig. 10-1 Push eight shock-absorbent pads to fasten HDD bracket.



Fig. 10-2 Fasten the screws to lock 2.5" HDD bracket and bracket together.

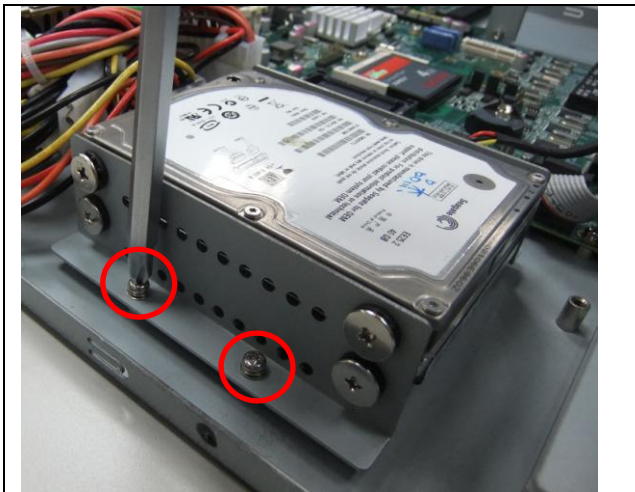


Fig. 10-3 Fix HDD bracket on chassis with four screws

Chapter 11 Installing Add-on Card



Fig. 11-1 Loosen screw on slot bracket.

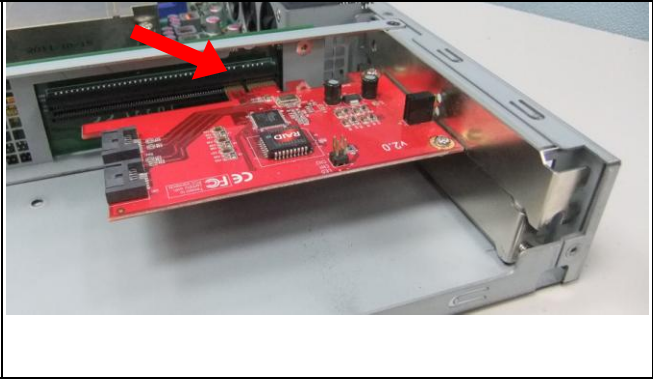


Fig. 11-2 Slide in PCI-e add-on card.

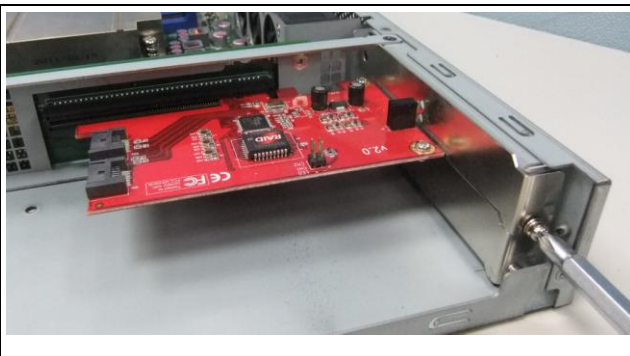


Fig. 11-3 Fix the add-on card

Chapter 12 Installing Mini PCI-e Card

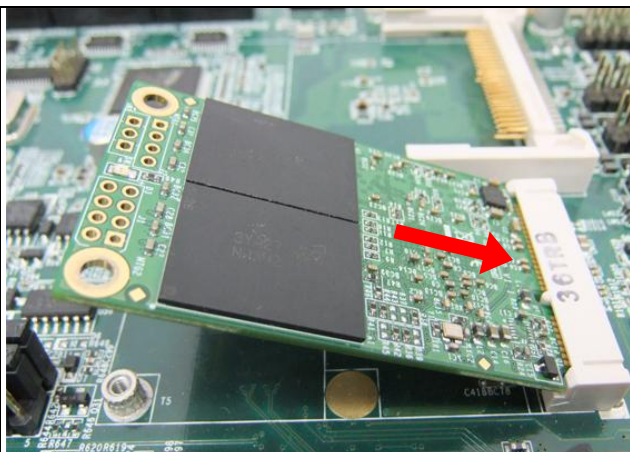


Fig. 12-1 Insert Mini PCI-e card.

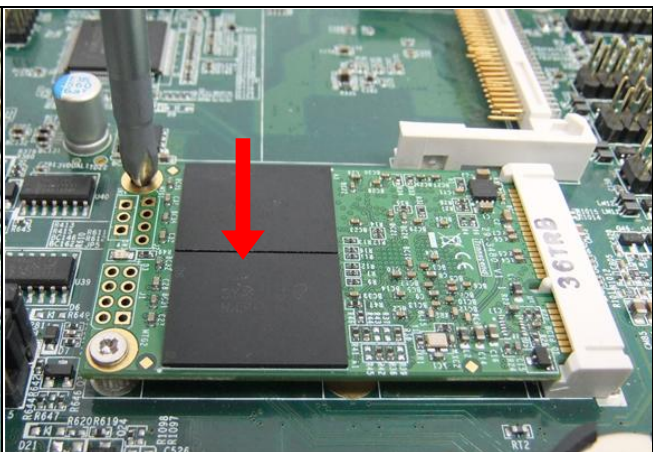


Fig. 12-2 Push down Mini PCI-e card & fix it with two M2 screws

Chapter 13 BIOS Information

This setup allows you to view processor configuration used in your computer system and set the system time and date.

Main Settings

Aptio Setup Utility – Copyright © 2012 American Megatrends, Inc.					
Main	Advanced	Chipset	Boot	Security	Save & Exit
BIOS Information				Choose the system default language	
System Language				[English]	→ ← Select Screen
System Date				[Fri 02/21/2014]	↑ ↓ Select Item
System Time				[10:30:55]	Enter: Select
Access Level				Administrator	+ - Change Field
				F1: General Help	
				F2: Previous Values	
				F3: Optimized Default	
				F4: Save ESC: Exit	

System Language

Choose the system default language.

System Date

Set the Date. Use Tab to switch between Data elements.

System Time

Set the Time. Use Tab to switch between Data elements.

Advanced Settings

This section allows you to configure and improve your system and allows you to set up some system features according to your preference.

Aptio Setup Utility					
Main	Advanced	Chipset	Boot	Security	Save & Exit
► PCI Subsystem Settings					
► ACPI Settings					
► Wake up event setting					
► CPU Configuration					
► SATA Configuration					
► Thermal Configuration					
► Shutdown Temperature Configuration					
► LAN Bypass Configuration					
► Intel(R) Rapid Start Technology					
► Intel TXT(LT) Configuration					
► Intel(R) Anti-Theft Technology Configura...					
► AMT Configuration					
► Acoustic Management Configuration					
► USB Configuration					
► F81866 Super IO Configuration					
► F81866 H/W Monitor					
► Serial Port Console Redirection					
				→ ← Select Screen	
				↑ ↓ Select Item	
				Enter: Select	
				+ - Change Field	
				F1: General Help	
				F2: Previous Values	
				F3: Optimized Default	
				F4: Save ESC: Exit	

PCI Subsystem Settings

Aptio Setup Utility					
Main	Advanced	Chipset	Boot	Security	Save & Exit
PCI Bus Driver Version			V 2.05.02		→ ← Select Screen
PCI Common Settings					↑ ↓ Select Item
PCI Latency Timer			[32 PCI Bus Clocks]		Enter: Select
VGA Palette Snoop			[Disabled]		+ - Change Field
PERR# Generation			[Disabled]		F1: General Help
SERR# Generation			[Disabled]		F2: Previous Values
					F3: Optimized Default
					F4: Save ESC: Exit
► PCI Express Settings					

PCI Latency Timer

Value to be programmed into PCI Latency Timer Register.

VGA Palette Snoop

Enables or disables VGA Palette Registers Snooping.

PERR# Generation

Enables or disables PCI device to generate PERR#.

SERR# Generation

Enables or disables PCI device to generate SERR#.

PCI Express Settings

Change PCI Express devices settings.

PCI Express Settings

Aptio Setup Utility					
Main	Advanced	Chipset	Boot	Security	Save & Exit
PCI Express Device Register Settings					→ ← Select Screen ↑ ↓ Select Item Enter: Select +- Change Field F1: General Help F2: Previous Values F3: Optimized Default F4: Save ESC: Exit
Relaxed Ordering			[Disabled]		
Extended Tag			[Disabled]		
No Snoop			[Enabled]		
Maximum Payload			[Auto]		
Maximum Read Request			[Auto]		
PCI Express Link Register Settings					
ASPM Support			[Disabled]		
WARNING: Enabling ASPM may cause some			PCI-E devices to fail		
Extended Synch			[Disabled]		
Link Training Retry			[5]		
Link Training Timeout			100		
Unpopulated Links			[Keep Link ON]		
Restore PCIE Register			[Disabled]		

Relaxed Ordering

Enables or disables PCI Express Device Relaxed Ordering.

Extended Tag

If ENABLED allows device to use 8-bit Tag field as a requester.

No Snoop

Enables or disables PCI Express Device No Snoop option.

Maximum Payload

Set Maximum Payload of PCI Express Device or allow System BIOS to select the value.

Maximum Read Request

Set Maximum Read Request Size of PCI Express Device or allow System BIOS to select the value.

ASPM Support

Set the ASPM Level: Force L0s – Force all links to L0s State:

AUTO – BIOS auto configure : DISABLE – Disables ASPM.

Extended Synch

If ENABLED allows generation of Extended Synchronization patterns.

Link Training Retry

Defines number of Retry Attempts software will take to retrain the link if previous training attempt was unsuccessful.

Link Training Timeout

Defines number of Microseconds software will wait before polling 'Link Training' bit in Link Status register. Value range from 10 to 1000 uS.

Unpopulated Links

In order to save power, software will disable unpopulated PCI Express links, if this option set to 'Disable Link'.

ACPI Settings

Aptio Setup Utility					
Main	Advanced	Chipset	Boot	Security	Save & Exit
ACPI Settings					
Enable ACPI Auto Conf			[Disabled]	→ ← Select Screen ↑ ↓ Select Item Enter: Select +- Change Field F1: General Help F2: Previous Values F3: Optimized Default F4: Save ESC: Exit	
Enable Hibernation			[Enabled]		
ACPI Sleep State			[S1 only (CPU Stop C...]		
Lock Legacy Resources			[Disabled]		
S3 Video Repost			[Disabled]		

Enable Hibernation

Enables or Disables System ability to Hibernate (OS/S4 Sleep State). This option may be not effective with some OS.

ACPI Sleep State

Select ACPI sleep state the system will enter, when the SUSPEND button is pressed.

Lock Legacy Resources

Enabled or Disabled Lock of Legacy Resources.

S3 Video Repost

Enable or disable S3 Video Repost.

Wake up event settings

Aptio Setup Utility					
Main	Advanced	Chipset	Boot	Security	Save & Exit
Wake system with Fixed Time			[Disabled]	→ ← Select Screen ↑ ↓ Select Item Enter: Select +- Change Field F1: General Help F2: Previous Values F3: Optimized Default F4: Save ESC: Exit	
Wake on Ring			[Enabled]		
Wake on PCI PME			[Enabled]		
Wake on PCIE Wake Event			[Enabled]		

Wake system with Fixed Time

Enables or Disables System wake on alarm event. When enabled, System will wake on the hr::min:: sec specified.

Wake on PCIE PME Wake Event

The options are Disabled and Enabled.

Trusted Computing

Aptio Setup Utility					
Main	Advanced	Chipset	Boot	Security	Save & Exit
Configuration					
Security Device Sup			[Disabled]	→ ← Select Screen ↑ ↓ Select Item Enter: Select +- Change Field F1: General Help F2: Previous Values F3: Optimized Default F4: Save ESC: Exit	
Current TPM Status Information					
SUPPORT TUREND OFF					

Security Device Support

Enables or disables BIOS support for security device. O.S. will not show Security Device. TCG EFI protocol and INT1A interface will not be available.

CPU Configuration

This section shows the CPU configuration parameters.

Aptio Setup Utility					
Main	Advanced	Chipset	Boot	Security	Save & Exit
CPU Configuration					
Intel(R) Xeon(R) CPU E3-1268L v3 @		2.30GHz			
CPU Signature		306c3			
Processor Family		6			
Microcode Patch		16			
FSB Speed		100 MHz			
Max CPU Speed		2300 MHz			
Min CPU Speed		800 MHz			
CPU Speed		2700 MHz			
Processor Cores		4			
Intel HT Technology		Supported			
Intel VT-x Technology		Supported			
Intel SMX Technology		Supported			
64-bit		Supported			
EIST Technology		Supported			
CPU C3 state		Supported			
CPU C6 state		Supported			
CPU C7 state		Supported			
L1 Data Cache		32 kB x 4			
L1 Code Cache		32 kB x 4			
L2 Cache		256 kB x 4			
L3 Cache		8192 kB			
Hyper-threading		[Enabled]			
Active Processor Cores		[All]			
Limit CPUID Maximum		[Disabled]			
Execute Disable Bit		[Enabled]			
Intel Virtualization		[Enabled]			
Hardware Prefetcher		[Enabled]			
Adjacent Cache Line Prefetch		[Enabled]			
CPU AEC		[Enabled]			

Hyper-threading

Enabled for Windows XP and Linux (OS optimized for Hyper-Threading Technology) and Disabled for other OS (OS not optimized for Hyper-Threading Technology). When Disabled, only one thread per enabled core is enabled.

Active Processor Cores

Number of cores to enable in each processor package.

Limit CPUID Maximum

Disabled for Windows XP.

Execute Disable Bit

XD can prevent certain classes of malicious buffer overflow attacks when combined with a supporting OS (Windows Server 2003 SP1, Windows XP SP2, SuSE Linux 9.2, Re33dHat Enterprise 3 Update 3.)

Intel Virtualization Technology

When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology.

Hardware Prefetcher

To turn on/off the Mid level Cache (L2) streamer Prefetcher.

Adjacent Cache Line Prefetch

To turn on/off prefetching of adjacent cache lines.

SATA Configuration

SATA Devices Configuration.

Aptio Setup Utility					
Main	Advanced	Chipset	Boot	Security	Save & Exit
SATA Controller(s)		[Enabled]		→ ← Select Screen ↑ ↓ Select Item Enter: Select + - Change Field F1: General Help F2: Previous Values F3: Optimized Default F4: Save ESC: Exit	
SATA Mode Selection		[AHCI]			
SATA Port0		Empty			
Software Preserve		Unknown			
SATA Port1		Empty			
Software Preserve		Unknown			
SATA Port2		Empty			
Software Preserve		Unknown			
SATA Port3		Empty			
Software Preserve		Unknown			
SATA Port4		Empty			
Software Preserve		Unknown			
SATA Port5		Empty			
Software Preserve		Unknown			

SATA Controller(s)

Enable / Disable Serial ATA Controller.

SATA Mode Selection

- (1) IDE Mode.
- (2) AHCI Mode.
- (3) RAID Mode.

Thermal Configuration

Aptio Setup Utility					
Main	Advanced	Chipset	Boot	Security	Save & Exit
► Platform Thermal Configuration					

Platform Thermal Configuration

Aptio Setup Utility					
Main	Advanced	Chipset	Boot	Security	Save & Exit
Platform Thermal Configuration					
Automatic Thermal Rep		[Enabled]			
Active Trip Point 0 F		100			
Active Trip Point 1		[55 C]			
Active Trip Point 1 F		75			
Passive TC1 Value		1			
Passive TC2 Value		5			
Passive TSP Value		10			
PCH Thermal Device				[Disabled]	

Automatic Thermal Reporting

Configure CRT, PSV and ACO automatically based on values recommended in BWG's thermal reporting for thermal management settings. Set to Disable for manual configuration.

Shutdown Temperature Configuration

Aptio Setup Utility					
Main	Advanced	Chipset	Boot	Security	Save & Exit
ACPI Shutdown Temperature		[Disabled]			

ACPI Shutdown Temperature

Set function Disabled or 70/75/80/85/90/95/100 °C

LAN Bypass Configuration

Aptio Setup Utility					
Main	Advanced	Chipset	Boot	Security	Save & Exit
LAN Bypass Configuration					
Bypass Quick Setting			[Normal]		

Bypass Quick Setting

Set LAN Bypass to Normal, Bypass, Firewall or Custom Define Mode

Normal mode: All LAN ports in NORMAL. When Watchdog monitor system hangs, software will initiates a system reboot.

Bypass mode: All LAN ports in BYPASS during power-off or watchdog initiates Bypass. System will not reboot.

Firewall mode: All LAN ports in BYPASS until software change it to NORMAL under OS. When watchdog monitors system hang, software will initiates a system reboot.

Custom Define mode: Customer defines watchdog reset, watchdog Bypass and power-off Bypass settings.

Aptio Setup Utility					
Main	Advanced	Chipset	Boot	Security	Save & Exit
LAN Bypass Configuration					
Bypass Quick Setting			[Custom Define]		
WDT Reset Signal			[Disabled]		
WDT Bypass Setting					
LAN5 LAN6 Bypass			[Normal]		
LAN7 LAN8 Bypass			[Normal]		
Ext LAN1 LAN2 Bypass			[Normal]		
Ext LAN3 LAN4 Bypass			[Normal]		
System OFF Bypass Setting					
LAN5 LAN6 Bypass			[Normal]		
LAN7 LAN8 Bypass			[Normal]		
Ext LAN1 LAN2 Bypass			[Normal]		
Ext LAN3 LAN4 Bypass			[Normal]		

Note: "Ext LAN Bypass" items only appear when extended IBASE LAN module card installed.

AMT Configuration

Aptio Setup Utility					
Main	Advanced	Chipset	Boot	Security	Save & Exit
Intel AMT			[Enabled]		
BIOS Hotkey Pressed			[Disabled]		
MEBx Selection Screen			[Disabled]		
Hide Un-Configure ME Confirmation			[Disabled]		
Un-Configure ME			[Disabled]		
Amt Wait Timer			0		
Disable ME			[Disabled]		
ASF			[Enabled]		
Activate Remote Assistance Process			[Disabled]		
USB Configure			[Enabled]		
PET Progress			[Enabled]		
AMT CIRA Timeout			0		
Watchdog			[Disabled]		
OS Timer			0		
BIOS Timer			0		

→ ← Select Screen
 ↑ ↓ Select Item
 Enter: Select
 +- Change Field
 F1: General Help
 F2: Previous Values
 F3: Optimized Default
 F4: Save ESC: Exit

AMT Configuration

Options are Enabled and Disabled.

Note: iAMT H/W is always enabled. This option just controls the BIOS extension execution. If enabled, this requires additional firmware in the SPI device.

Unconfigure ME

Perform AMT/ME unconfigure without password operation.

Amt Wait Timer

Set timer to wait before sending ASF_GET_BOOT_OPTIONS.

Activate Remote Assistance Process

Trigger CIRA boot.

PET Progress

User can Enable/Disable PET Events progress to receive PET events or not.

Watchdog Timer

Enable/Disable Watchdog Timer.

Acoustic Management Configuration

Aptio Setup Utility					
Main	Advanced	Chipset	Boot	Security	Save & Exit
Acoustic Management Configuration				→ ← Select Screen ↑ ↓ Select Item Enter: Select +- Change Field F1: General Help F2: Previous Values F3: Optimized Default F4: Save ESC: Exit	
Automatic Acoustic Management		[Disabled]			

Smart fan function Enable or Disable.

USB Configuration

Aptio Setup Utility					
Main	Advanced	Chipset	Boot	Security	Save & Exit
USB Configuration					→ ← Select Screen ↑ ↓ Select Item Enter: Select +- Change Field F1: General Help F2: Previous Values F3: Optimized Default F4: Save ESC: Exit
USB Devices: 1 Keyboard, 1 Mouse, 2 Hubs					
Legacy USB Support			[Enabled]		
USB3.0 Support			[Enabled]		
XHCI Hand-off			[Enabled]		
EHCI Hand-off			[Disabled]		
Port 60/64 Emulation			[Enabled]		
USB hardware delays and time-outs:					
USB Transfer time-out			[20 sec]		
Device reset time-out			[20 sec]		
Device power-up delay			[Auto]		

Legacy USB Support

Enables Legacy USB support.

AUTO option disables legacy support if no USB devices are connected.

DISABLE option will keep USB devices available only for EFI applications.

USB3.0 Support

Enable/Disable USB3.0 (XHCI) Controller support.

XHCI Hand-off

This is a workaround for OSeS without XHCI hand-off support. The XHCI ownership change should be claimed by XHCI driver.

EHCI Hand-off

Enabled/Disabled. This is a workaround for OSeS without EHCI hand-off support. The EHCI ownership change should be claimed by EHCI driver.

Port 64/60 Emulation

Enables I/O port 60h/64h emulation support. This should be enabled for the complete USB keyboard legacy support for non-USB aware OSeS.

USB Transfer time-out

The time-out value for Control, Bulk, and Interrupt transfers.

Device reset time-out

USB mass Storage device start Unit command time-out.

Device power-up delay

Maximum time the device will take before it properly reports itself to the Host Controller. 'Auto' uses default value: for a Root port it is 100ms, for a Hub port the delay is taken from Hub descriptor.

F81866 Super IO Configuration

Aptio Setup Utility					
Main	Advanced	Chipset	Boot	Security	Save & Exit
Super IO Configuration					
F81866 Super IO Chip		F81866		→ ← Select Screen	
► Serial Port 0 Configuration				↑ ↓ Select Item	
► Serial Port 1 Configuration				Enter: Select	
Power Failure		[Always off]		+- Change Field	
KB/MS Power On		[None]		F1: General Help	
				F2: Previous Values	
				F3: Optimized Default	
				F4: Save ESC: Exit	

Serial Port Configuration

Set Parameters of Serial Ports. User can Enable/Disable the serial port and Select an optimal settings for the Super IO Device.

F81866 H/W Monitor

Aptio Setup Utility					
Main	Advanced	Chipset	Boot	Security	Save & Exit
PC Health Status				→ ← Select Screen ↑ ↓ Select Item Enter: Select +- Change Field F1: General Help F2: Previous Values F3: Optimized Default F4: Save ESC: Exit	
Fan1 smart fan control		[50 C]			
Fan2 smart fan control		[50 C]			
Fan3 smart fan control		[Disabled]			
System temperature1		+41 C			
System temperature2		+38 C			
System temperature3		+37 C			
FAN1 Speed		1545 RPM			
FAN2 Speed		1550 RPM			
FAN3 Speed		1546 RPM			
VIN1		+1.776 V			
VIN2		+5.171 V			
VIN3		+12.408 V			
VSB5V		+5.016 V			
VCC3V		+3.392 V			
VSB3V		+3.392 V			
VBAT		+3.264 V			

Temperatures/Voltages

These fields are the parameters of the hardware monitoring function feature of the motherboard. The values are read-only values as monitored by the system and show the PC health status.

Fan1/Fan2/Fan3 Smart Fan Control

This field enables or disables the smart fan feature. At a certain temperature, the fan starts turning. Once the temperature drops to a certain level, it stops turning again.

Chipset Settings

This section allows you to configure and improve your system and allows you to set up some system features according to your preference.

Aptio Setup Utility					
Main	Advanced	Chipset	Boot	Security	Save & Exit
▶ PCH-IO Configuration ▶ System Agent (SA) Configuration					→ ←Select Screen ↑ ↓ Select Item Enter: Select + - Change Field F1: General Help F2: Previous Values F3: Optimized Default F4: Save ESC: Exit

PCH-IO Configuration

This section allows you to configure the North Bridge Chipset.

Aptio Setup Utility					
Main	Advanced	Chipset	Boot	Security	Save & Exit
			Intel PCH RC Version	1.6.2.0	
			Intel PCH SKU Name	C226	
			Intel PCH Rev ID	O5/C2	
			▶ PCI Express Configuration		
			▶ USB Configuration		
			▶ PCH Azalia Configuration		
			▶ BIOS Security Configuration		
			PCH LAN Controller	[Enabled]	→ ← Select Screen
			Wake on LAN	[Enabled]	↑ ↓ Select Item
			DeepSx Power Policies	[Disabled]	Enter: Select
			Display Logic	[Enabled]	+ - Change Field
			CLKRUN# Logic	[Enabled]	F1: General Help
			SB CRID	[Disabled]	F2: Previous Values
			SLP_S4 Assertion Width	[4-5 Seconds]	F3: Optimized Default
			Restore AC Power Loss	[Last State]	F4: Save ESC: Exit

PCH LAN Controller

Enable or disable onboard NIC.

Wake on LAN

Enable or disable integrated LAN to wake the system. (The Wake On LAN cannot be disabled if ME is on at Sx state.)

SLP_S4 Assertion Width

Select a minimum assertion width of the SLP_S4# signal.

Restore AC Power Loss

Select AC power state when power is re-applied after a power failure.

PCI Express Configuration

Main	Advanced	Chipset	Boot	Security	Save & Exit
			PCI Express Configuration		
			PCI Express Clock Gating	[Enabled]	
			DMI Link ASPM Control	[Enabled]	
			DMI Link Extended Synch Control	[Disabled]	
			PCI Express Root Port Function	[Disabled]	
			Subtractive Decode	[Disabled]	
			PCI Express Port 1 is assign		
			▶ PCI Express Root Port 2		
			▶ PCI Express Root Port 3		
			▶ PCI Express Root Port 4		
			▶ PCI Express Root Port 5		
			▶ PCI Express Root Port 6		
			▶ PCI Express Root Port 7		
			▶ PCI Express Root Port 8		
			→ ← Select Screen		
			↑ ↓ Select Item		
			Enter: Select		
			+ - Change Field		
			F1: General Help		
			F2: Previous Values		
			F3: Optimized Default		
			F4: Save ESC: Exit		

PCI Express Clock Gating

Enable or disable PCI Express Clock Gating for each root port.

DMI Link ASPM Control

The control of Active State Power Management on both NB side and SB side of the DMI link.

PCI Express Root Port Function

Enable or disable PCI express Root Port function swapping.

USB Configuration

Main	Advanced	Chipset	Boot	Security	Save & Exit
USB Configuration					
USB Precondition			[Disabled]		→ ← Select Screen
XHCI Mode			[Smart Auto]		↑ ↓ Select Item
BTCG			[Enable]		Enter: Select
USB Ports Per-Port Disable Control			[Disabled]		+ - Change Field
					F1: General Help
					F2: Previous Values
					F3: Optimized Default
					F4: Save ESC: Exit

USB Precondition

Precondition work on USB host controller and root ports for faster enumeration.

xHCI Mode

Mode of operation of xHCI controller

BTCG

Enable or disable trunk clock gating.

USB Ports Per-Port Disable Control

Control each of the USB ports (0~13) disabling.

PCH Azalia Configuration

Main	Advanced	Chipset	Boot	Security	Save & Exit
PCH Azalia Configuration					
Azalia			[Auto]		→ ← Select Screen
Azalia Docking Support			[Disabled]		↑ ↓ Select Item
Azalia PME			[Disabled]		Enter: Select
					+ - Change Field
					F1: General Help
					F2: Previous Values
					F3: Optimized Default
					F4: Save ESC: Exit

Azalia

Control Detection of the Azalia device.

Disabled = Azalia will unconditionally disabled.

Enabled Azalia will be unconditionally enabled.

Auto = Azalia will enabled if present, disabled otherwise.

System Agent (SA) Configuration

Aptio Setup Utility					
Main	Advanced	Chipset	Boot	Security	Save & Exit
System Agent Bridge Name			Haswell		
System Agent RC Version			1.6.2.0		
VT-d Capability			Supported		
VT-d			[Enabled]		
CHAP Device (B0:D7:F0)			[Disabled]		→ ← Select Screen
Thermal Device (B0:D4:F0)			[Disabled]		↑ ↓ Select Item
Enable NB CRID			[Disabled]		Enter: Select
BDAT ACPI Table Support			[Disabled]		+ - Change Field
► Graphics Configuration					F1: General Help
► DMI Configuration					F2: Previous Values
► NB PCIe Configuration					F3: Optimized Default
► Memory Configuration					F4: Save ESC: Exit
► Memory Thermal Configuration					
► GT – Power Management Control					

VT-d

Check to enable VT-d function on MCH.

Enable NB CRID

Enable or disable NB CRID WorkAround.

Graphics Configuration

Aptio Setup Utility					
Main	Advanced	Chipset	Boot	Security	Save & Exit
Graphics Configuration					
IGFX VBIOS Version			2164		
IGfx Frequency			700 MHz		
Graphics Turbo IMON			31		
Primary Display			[Auto]		→ ← Select Screen
Internal Graphics			[Auto]		↑ ↓ Select Item
GTT Size			[2MB]		Enter: Select
Aperture Size			[256MB]		+ - Change Field
DVMT Pre-Allocated			[32M]		F1: General Help
DVMT Total Gfx Mode			[256M]		F2: Previous Values
Gfx Low Power Mode			[Enabled]		F3: Optimized Default
Graphics Performance			[Disabled]		F4: Save ESC: Exit
▶ LCD Control					

Primary Display

Select which of IGFX/PEG/PCI graphics device should be primary display or select SG for switchable Gfx.

Internal Graphics

Keep IGD enabled based on the setup options.

DVMT Pre-Allocated

Select DVMT 5.0 Pre-Allocated (Fixed) graphics memory size used by the internal graphics device.

DVMT Total Gfx Mem

Select DVMT 5.0 total graphics memory size used by the internal graphics device.

Gfx Low Power Mode

This option is applicable for SFF only.

Primary IGFX Boot Display (LCD Control)

Select the Video Device that will be activated during POST. This has no effect if external graphics present.

Secondary boot display selection will appear based on your selection. VGA modes will be supported only on primary display.

Memory Configuration

Aptio Setup Utility					
Main	Advanced	Chipset	Boot	Security	Save & Exit
Memory Information					
Memory Frequency			1600 MHz		
Total Memory			32768 MB (DDR3)		
DIMM#0			8192 MB (DDR3)		
DIMM#1			8192 MB (DDR3)		→ ← Select Screen
DIMM#2			8192 MB (DDR3)		↑ ↓ Select Item
DIMM#3			8192 MB (DDR3)		Enter: Select
CAS Latency (tCL)			11		+ - Change Field
Minimum delay time					F1: General Help
CAS to RAS (tRCDmin)			11		F2: Previous Values
Row Precharge (tRPmin)			11		F3: Optimized Default
Active to Precharge (tRASmin)			28		F4: Save ESC: Exit
XMP Profile 1			Not Supported		
XMP Profile 2			Not Supported		

Boot Settings

Aptio Setup Utility					
Main	Advanced	Chipset	Boot	Security	Save & Exit
Boot Configuration			1		
Setup Prompt Timeout			[On]		
Bootup NumLock State			[Disabled]		
Quiet Boot			[Disabled]		
Fast Boot			[Disabled]		
Boot mode select			[LEGACY]		→ ← Select Screen
FIXED BOOT ORDER Priorities					↑ ↓ Select Item
Boot Option #1			[Hard Disk]		Enter: Select
Boot Option #2			[CD/DVD]		+ - Change Field
Boot Option #3			[USB Hard Disk]		F1: General Help
Boot Option #4			[USB CD/DVD]		F2: Previous Values
Boot Option #5			[USB Key]		F3: Optimized Default
Boot Option #6			[USB Floppy]		F4: Save ESC: Exit
Boot Option #7			[Network]		
► CSM16 parameters					

Setup Prompt Timeout

Number of seconds to wait for setup activation key.
65535(0xFFFF) means indefinite waiting.

Bootup NumLock State

Select the keyboard NumLock state.

Quiet Boot

Enables/Disables Quiet Boot option.

Fast Boot

Enables/Disables boot with initialization of a minimal set of devices required to launch active boot option. Has no effect for BBS boot options.

Boot Option Priorities

Sets the system boot order.

CSM16 parameters

This section allows you to configure the boot settings.

Aptio Setup Utility					
Main	Advanced	Chipset	Boot	Security	Save & Exit
CSM16 Parameters					
CSM16 Module Version			07.70		→ ← Select Screen
GateA20 Active			[Upon Request]		↑ ↓ Select Item
Option ROM Messages			[Force BIOS]		Enter: Select
INT19 Trap Response			[Immediate]		+ - Change Field
					F1: General Help
					F2: Previous Values
					F3: Optimized Default
					F4: Save ESC: Exit

GateA20 Active

UPON REQUEST: GA20 can be disabled using BIOS services

ALWAYS: do not allow disabling GA20; this option is useful when any RT code is executed above 1MB.

Option ROM Messages

Set display mode for Option ROM

INT19 Trap Response

BIOS reaction on INT19 trapping by option ROM:

IMMEDIATE: execute the trap right away.

POSTPONED: execute the trap during legacy boot.

Security Settings

This section allows you to configure and improve your system and allows you to set up some system features according to your preference.

Aptio Setup Utility					
Main	Advanced	Chipset	Boot	Security	Save & Exit
Password Description					
If ONLY the Administrator's password is set, then this only limit access to Setup and is only asked for when entering Setup. If ONLY the User's password is set, then this is a power on password and must be entered to boot or enter Setup. In Setup the User will have Administrator rights The password length must be in the following range:					
Minimum length				3	
Maximum length				20	
Administrator Password					
User Password					
				→ ← Select Screen ↑ ↓ Select Item Enter: Select +- Change Field F1: General Help F2: Previous Values F3: Optimized Default F4: Save ESC: Exit	

Administrator Password

Set Setup Administrator Password.

User Password

Set User Password.

Save & Exit Settings

Aptio Setup Utility					
Main	Advanced	Chipset	Boot	Security	Save & Exit
Save Changes and Exit					
Discard Changes and Exit					
Save Changes and Reset					
Discard Changes and Reset					
Save Options					
Save Changes					
Discard Changes					
Restore Defaults					
Save as User Defaults					
Restore User Defaults					
Boot Override					
Launch EFI Shell from filesystem device					
				→ ← Select Screen ↑ ↓ Select Item Enter: Select +- Change Field F1: General Help F2: Previous Values F3: Optimized Default F4: Save ESC: Exit	

Save Changes and Exit

Exit system setup after saving the changes.

Discard Changes and Exit

Exit system setup without saving any changes.

Save Changes and Reset

Reset the system after saving the changes.

Discard Changes and Reset

Reset system setup without saving any changes.

Save Changes

Save Changes done so far to any of the setup options.

Discard Changes

Discard Changes done so far to any of the setup options.

Restore Defaults

Restore/Load Defaults values for all the setup options.

Save as User Defaults

Save the changes done so far as User Defaults.

Restore User Defaults

Restore the User Defaults to all the setup options.

Chapter 14 Watchdog Timer Configuration

The WDT is used to generate a variety of output signals after a user programmable count. The WDT is suitable for use in the prevention of system lock-up, such as when software becomes trapped in a deadlock. Under these sorts of circumstances, the timer will count to zero and the selected outputs will be driven. Under normal circumstance, the user will restart the WDT at regular intervals before the timer counts to zero.

SAMPLE CODE:

This code and information is provided "as is" without warranty of any kind, either expressed or implied, including but not limited to the implied warranties of merchantability and/or fitness for a particular purpose.

```
//-----  
//  
// THIS CODE AND INFORMATION IS PROVIDED "AS IS" WITHOUT WARRANTY OF ANY  
// KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE  
// IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A PARTICULAR  
// PURPOSE.  
//  
//-----  
#include <dos.h>  
#include <conio.h>  
#include <stdio.h>  
#include <stdlib.h>  
#include "F81866.H"  
//-----  
int main (int argc, char *argv[]);  
void EnableWDT(int);  
void DisableWDT(void);  
//-----  
int main (int argc, char *argv[])  
{  
    unsigned char bBuf;  
    unsigned char bTime;  
    char **endptr;  
  
    char SIO;  
  
    printf("Fintek 81866 watch dog program\n");  
  
    SIO = Init_F81866();  
    if (SIO == 0)  
    {  
        printf("Can not detect Fintek 81866, program abort.\n");  
        return(1);  
    }  
    if (SIO == 0)  
  
    if (argc != 2)  
    {  
        printf(" Parameter incorrect!!\n");  
        return (1);  
    }  
  
    bTime = strtol (argv[1], endptr, 10);  
    printf("System will reset after %d seconds\n", bTime);  
  
    if (bTime)  
    {  
        EnableWDT(bTime);  
    }  
    else  
    {  
        DisableWDT();  
    }  
}
```

```

        return 0;
    }

//-----
void EnableWDT(int interval)
{
    unsigned char bBuf;

    bBuf = Get_F81866_Reg(0x2B);
    bBuf &= (~0x20);
    Set_F81866_Reg(0x2B, bBuf);                //Enable WDTO

    Set_F81866_LD(0x07);                        //switch to logic device 7
    Set_F81866_Reg(0x30, 0x01);                //enable timer

    bBuf = Get_F81866_Reg(0xF5);
    bBuf &= (~0x0F);
    bBuf |= 0x52;
    Set_F81866_Reg(0xF5, bBuf);                //count mode is second

    Set_F81866_Reg(0xF6, interval);            //set timer

    bBuf = Get_F81866_Reg(0xFA);
    bBuf |= 0x01;
    Set_F81866_Reg(0xFA, bBuf);                //enable WDTO output

    bBuf = Get_F81866_Reg(0xF5);
    bBuf |= 0x20;
    Set_F81866_Reg(0xF5, bBuf);                //start counting
}
//-----
void DisableWDT(void)
{
    unsigned char bBuf;

    Set_F81866_LD(0x07);                        //switch to logic device 7

    bBuf = Get_F81866_Reg(0xFA);
    bBuf &= ~0x01;
    Set_F81866_Reg(0xFA, bBuf);                //disable WDTO output

    bBuf = Get_F81866_Reg(0xF5);
    bBuf &= ~0x20;
    bBuf |= 0x40;
    Set_F81866_Reg(0xF5, bBuf);                //disable WDT
}
//-----
//-----
//
// THIS CODE AND INFORMATION IS PROVIDED "AS IS" WITHOUT WARRANTY OF ANY
// KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE
// IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A PARTICULAR
// PURPOSE.
//
//-----
#include "F81866.H"
#include <dos.h>
//-----
unsigned int F81866_BASE;
void Unlock_F81866 (void);
void Lock_F81866 (void);
//-----
unsigned int Init_F81866(void)
{
    unsigned int result;
    unsigned char ucDid;

    F81866_BASE = 0x4E;
    result = F81866_BASE;

```

```

    ucDid = Get_F81866_Reg(0x20);
    if (ucDid == 0x07)
    {
        goto Init_Finish; }

    F81866_BASE = 0x2E;
    result = F81866_BASE;
    ucDid = Get_F81866_Reg(0x20);
    if (ucDid == 0x07)
    {
        goto Init_Finish; }

    F81866_BASE = 0x00;
    result = F81866_BASE;

Init_Finish:
    return (result);
}
//-----
void Unlock_F81866 (void)
{
    outportb(F81866_INDEX_PORT, F81866_UNLOCK);
    outportb(F81866_INDEX_PORT, F81866_UNLOCK);
}
//-----
void Lock_F81866 (void)
{
    outportb(F81866_INDEX_PORT, F81866_LOCK);
}
//-----
void Set_F81866_LD( unsigned char LD)
{
    Unlock_F81866();
    outportb(F81866_INDEX_PORT, F81866_REG_LD);
    outportb(F81866_DATA_PORT, LD);
    Lock_F81866();
}
//-----
void Set_F81866_Reg( unsigned char REG, unsigned char DATA)
{
    Unlock_F81866();
    outportb(F81866_INDEX_PORT, REG);
    outportb(F81866_DATA_PORT, DATA);
    Lock_F81866();
}
//-----
unsigned char Get_F81866_Reg(unsigned char REG)
{
    unsigned char Result;
    Unlock_F81866();
    outportb(F81866_INDEX_PORT, REG);
    Result = inportb(F81866_DATA_PORT);
    Lock_F81866();
    return Result;
}
//-----
//-----
//
// THIS CODE AND INFORMATION IS PROVIDED "AS IS" WITHOUT WARRANTY OF ANY
// KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE
// IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A PARTICULAR
// PURPOSE.
//
//-----
#ifndef __F81866_H
#define __F81866_H 1
//-----
#define F81866_INDEX_PORT (F81866_BASE)
#define F81866_DATA_PORT (F81866_BASE+1)
//-----
#define F81866_REG_LD 0x07
//-----

```

```

#define F81866_UNLOCK                0x87
#define F81866_LOCK                  0xAA
//-----
unsigned int Init_F81866(void);
void Set_F81866_LD( unsigned char);
void Set_F81866_Reg( unsigned char, unsigned char);
unsigned char Get_F81866_Reg( unsigned char);
//-----
#endif  __F81866_H

```

Chapter 15 Digital I/O Sample Configuration

Filename : Main.cpp

```

//-----
//
// THIS CODE AND INFORMATION IS PROVIDED "AS IS" WITHOUT WARRANTY OF ANY
// KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE
// IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A PARTICULAR
// PURPOSE.
//
//-----
#include <dos.h>
#include <conio.h>
#include <stdio.h>
#include <stdlib.h>
#include "F81865.H"

#define BIT0 0x01
#define BIT1 0x02
#define BIT2 0x04
#define BIT3 0x08
#define BIT4 0x10
#define BIT5 0x20
#define BIT6 0x40
#define BIT7 0x80

//-----
int main (void);

void Dio5Initial(void);
void Dio5SetOutput(unsigned char);
unsigned char Dio5GetInput(void);
void Dio5SetDirection(unsigned char);
unsigned char Dio5GetDirection(void);
//-----
int main (void)
{
    char SIO;
    unsigned char DIO;

    printf("Fintek 81865/81866 digital I/O test program\n");

    SIO = Init_F81865();
    if (SIO == 0)
    {
        printf("Can not detect Fintek 81865/81866, program abort.\n");
        return(1);
    }
    if (SIO == 0)

    Dio5Initial();

/*
    //for GPIO50..57
    Dio5SetDirection(0xF0); //GP50..53 = input, GP54..57=output
    printf("Current DIO direction = 0x%X\n", Dio5GetDirection());

    printf("Current DIO status = 0x%X\n", Dio5GetInput());

    printf("Set DIO output to high\n");
    Dio5SetOutput(0x0F);

    printf("Set DIO output to low\n");
    Dio5SetOutput(0x00);
*/

    //for GPIO50..57
    Dio5SetDirection(0xF0); //GP50..53 = input, GP54..57=output

    Dio5SetOutput(0x00); //clear
    DIO = Dio5GetInput() & 0x0F;

```

```

Dio5SetOutput(0x00);                                //clear
DIO = Dio5GetInput() & 0x0F;
if (DIO != 0x0A)
{
    printf("The Fintek 81865 digital IO abnormal, abort.\n");
    return(1);
}
Dio5SetOutput(0xA0);                                //clr# is high
Dio5SetOutput(0xF0);                                //clk and clr# is high
Dio5SetOutput(0xA0);                                //clr# is high

DIO = Dio5GetInput() & 0x0F;
if (DIO != 0x05)
{
    printf("The Fintek 81865 digital IO abnormal, abort.\n");
    return(1);
}
printf("!!! Pass !!!\n");
return 0;
}
//-----
void Dio5Initial(void)
{
    unsigned char ucBuf;

    //switch GPIO multi-function pin for      gpio 50~57

//gpio53~57 UR5_FULL_EN(bit1), clear UR6_FULL_EN(bit3)
//set UR5_FULL_EN, should set UR_GP_PROG_EN = 1 (reg26, bit0) first

    ucBuf = Get_F81865_Reg(0x26);
    ucBuf |= BIT0;
    Set_F81865_Reg(0x26, ucBuf);
    //set UR5_FULL_EN(bit1), clear UR6_FULL_EN(bit3)
    ucBuf = Get_F81865_Reg(0x2A);
    ucBuf &= ~BIT3; //clear bit 3,
    ucBuf |= BIT1; //set bit 1,
    Set_F81865_Reg(0x2a, ucBuf);

//GPIO51 ~ GPIO52
    //clear UR6_ALT_EN(bit5), IR_ALT_EN(bit4), set FDC_GP_EN(bit3)

//GPIO50
//set FDC_GP_EN(bit3), clear RTS6_ALT_EN(RTS6_2_ALT_EN)(bit6)

    ucBuf = Get_F81865_Reg(0x2A);
    ucBuf &= ~(BIT4+BIT5+BIT6); //clear UR6_ALT_EN(bit5), IR_ALT_EN(bit4), RTS6_ALT_EN(RTS6_2_ALT_EN)(bit6)
    Set_F81865_Reg(0x2a, ucBuf);
    //set FDC_GP_EN(bit3), should clear UR_GP_PROG_EN (reg26, bit0) first
    ucBuf = Get_F81865_Reg(0x26);
    ucBuf &= ~BIT0;
    Set_F81865_Reg(0x26, ucBuf); //clear UR_GP_PROG_EN = 0 (reg26, bit0)

    ucBuf = Get_F81865_Reg(0x2A);
    ucBuf |= BIT3; //set FDC_GP_EN(bit3),
    Set_F81865_Reg(0x2a, ucBuf);

    Set_F81865_LD(0x06); //switch to logic device 6

    //enable the GP5 group
    ucBuf = Get_F81865_Reg(0x30);
    ucBuf |= 0x01;
    Set_F81865_Reg(0x30, ucBuf);

    Set_F81865_Reg(0xA0, 0x00); //define as input mode
    Set_F81865_Reg(0xA3, 0xFF); //push pull mode
}
//-----

```

```

void Dio5SetOutput(unsigned char NewData)
{
    Set_F81865_LD(0x06);
    Set_F81865_Reg(0xA1, NewData);
}
//-----
unsigned char Dio5GetInput(void)
{
    unsigned char result;

    Set_F81865_LD(0x06);
    result = Get_F81865_Reg(0xA2);
    return (result);
}
//-----
void Dio5SetDirection(unsigned char NewData)
{
    //NewData : 1 for input, 0 for output
    Set_F81865_LD(0x06);
    Set_F81865_Reg(0xA0, NewData);
}
//-----
unsigned char Dio5GetDirection(void)
{
    unsigned char result;

    Set_F81865_LD(0x06);
    result = Get_F81865_Reg(0xA0);
    return (result);
}
//-----

```

Filename : 81865.cpp

```

//-----
//
// THIS CODE AND INFORMATION IS PROVIDED "AS IS" WITHOUT WARRANTY OF ANY
// KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE
// IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A PARTICULAR
// PURPOSE.
//
//-----
#include "F81865.H"
#include <dos.h>
//-----
unsigned int F81865_BASE;
void Unlock_F81865 (void);
void Lock_F81865 (void);
//-----
unsigned int Init_F81865(void)
{
    unsigned int result;
    unsigned char ucDid;

    F81865_BASE = 0x4E;
    result = F81865_BASE;

    ucDid = Get_F81865_Reg(0x20);
    if (ucDid == 0x07||ucDid == 0x10)
    {
        goto Init_Finish;
    }

    F81865_BASE = 0x2E;
    result = F81865_BASE;

    ucDid = Get_F81865_Reg(0x20);
    if (ucDid == 0x07||ucDid == 0x10)
    {
        goto Init_Finish;
    }

    F81865_BASE = 0x00;
    result = F81865_BASE;

Init_Finish:
    return (result);
}
//-----
void Unlock_F81865 (void)
{
    outportb(F81865_INDEX_PORT, F81865_UNLOCK);
    outportb(F81865_INDEX_PORT, F81865_UNLOCK);
}
//-----
void Lock_F81865 (void)
{
    outportb(F81865_INDEX_PORT, F81865_LOCK);
}
//-----
void Set_F81865_LD( unsigned char LD)
{
    Unlock_F81865();
    outportb(F81865_INDEX_PORT, F81865_REG_LD);
    outportb(F81865_DATA_PORT, LD);
    Lock_F81865();
}
//-----
void Set_F81865_Reg( unsigned char REG, unsigned char DATA)
{
    Unlock_F81865();
    outportb(F81865_INDEX_PORT, REG);
    outportb(F81865_DATA_PORT, DATA);
    Lock_F81865();
}
//-----
unsigned char Get_F81865_Reg(unsigned char REG)
{
    unsigned char Result;

```

```

        Unlock_F81865();
        outportb(F81865_INDEX_PORT, REG);
        Result = inportb(F81865_DATA_PORT);
        Lock_F81865();
        return Result;
    }
//-----

```

Filename : 81865.h

```

//-----
//
// THIS CODE AND INFORMATION IS PROVIDED "AS IS" WITHOUT WARRANTY OF ANY
// KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE
// IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A PARTICULAR
// PURPOSE.
//
//-----
#ifndef __F81865_H
#define __F81865_H                                1
//-----
#define F81865_INDEX_PORT        (F81865_BASE)
#define F81865_DATA_PORT        (F81865_BASE+1)
//-----
#define F81865_REG_LD            0x07
//-----
#define F81865_UNLOCK            0x87
#define F81865_LOCK              0xAA
//-----
unsigned int Init_F81865(void);
void Set_F81865_LD( unsigned char);
void Set_F81865_Reg( unsigned char, unsigned char);
unsigned char Get_F81865_Reg( unsigned char);
//-----
#endif      // __F81865_H

```

This section describes the installation procedures for software and drivers under the Windows. The software and drivers are included with the board. If you find the items missing, please contact the vendor where you made the purchase. The contents of this section include the following:

Intel® Chipset Software Installation Utility
Intel® Graphics Driver Installation
LAN Drivers Installation
Intel® Management Engine Interface

IMPORTANT NOTE:

After installing your Windows operating system, you must install first the Intel® Chipset Software Installation Utility before proceeding with the drivers installation.

Intel® Chipset Software Installation Utility

The Intel Chipset Drivers should be installed first before the software drivers to enable Plug & Play INF support for Intel chipset components. Follow the instructions below to complete the installation.

1. Insert the CD that comes with the board. Click Intel and then Intel(R) 7 Series Chipset Drivers.



2. Click **Intel(R) Chipset Software Installation Utility**.



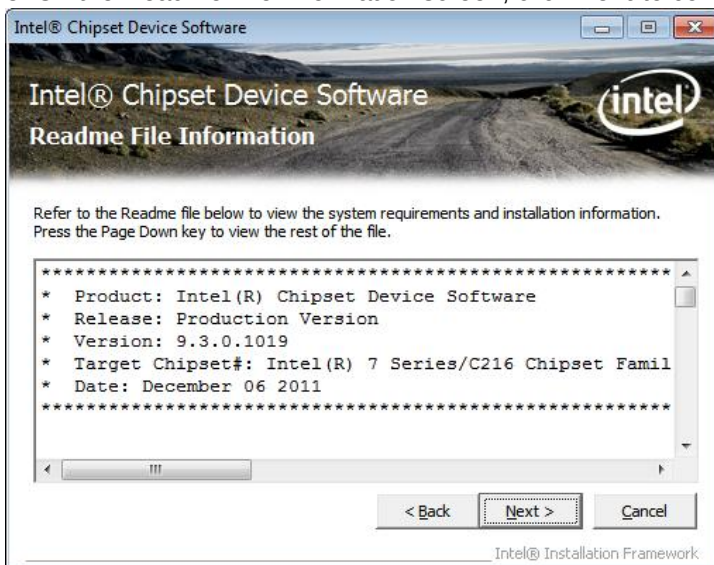
3. When the Welcome screen to the Intel® Chipset Device Software appears, click **Next** to continue.



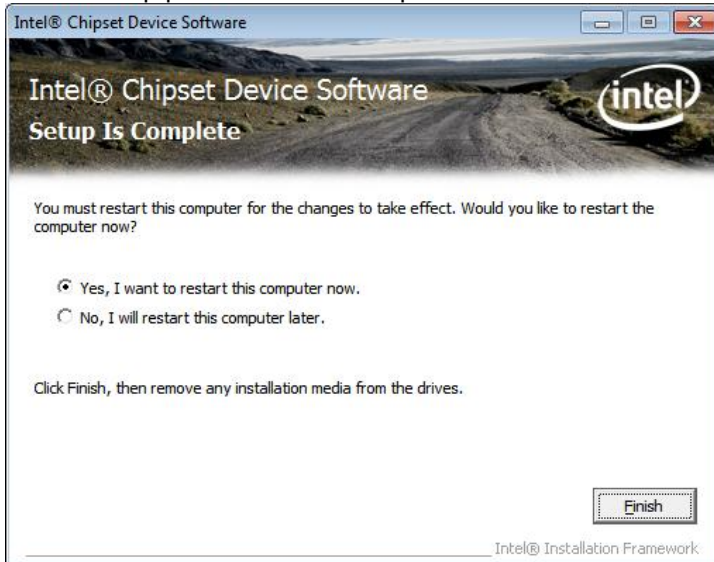
4. Click **Yes** to accept the software license agreement and proceed with the installation process.



5. On the Readme File Information screen, click **Next** to continue the installation.



6. The Setup process is now complete. Click **Finish** to restart the computer and for changes to take effect.



VGA Drivers Installation

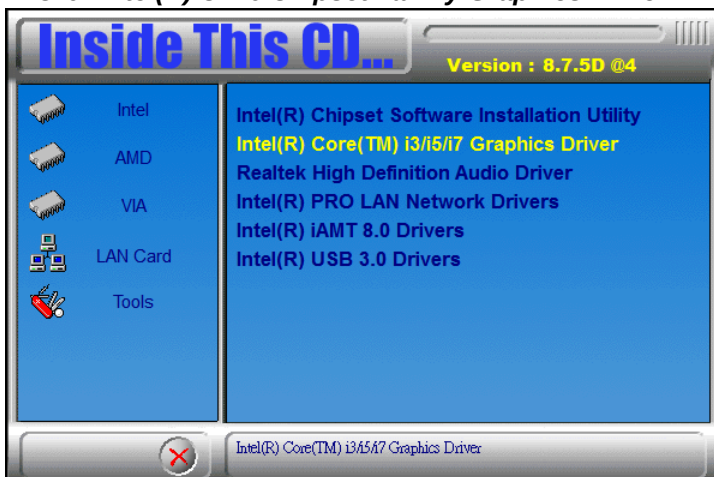
NOTE: Before installing the *Intel(R) C216 Chipset Family Graphics Driver*, the Microsoft .NET Framework 3.5 SPI should be first installed.

To install the VGA drivers, follow the steps below.

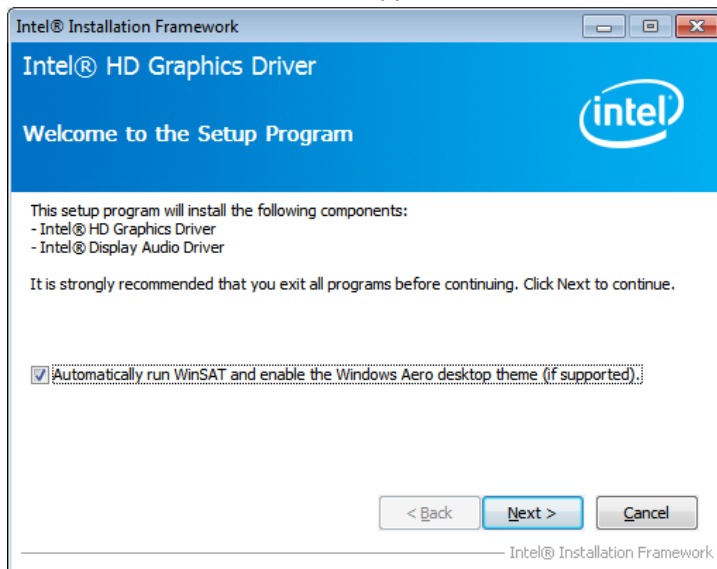
1. Insert the CD that comes with the board. Click **Intel** and then **Intel(R) Q7 Series Chipset Drivers**.



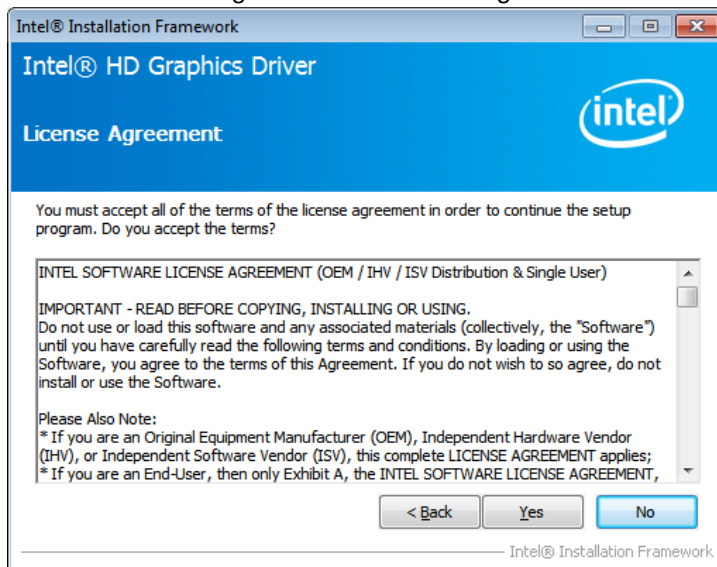
2. Click **Intel(R) C216 Chipset Family Graphics Driver**.



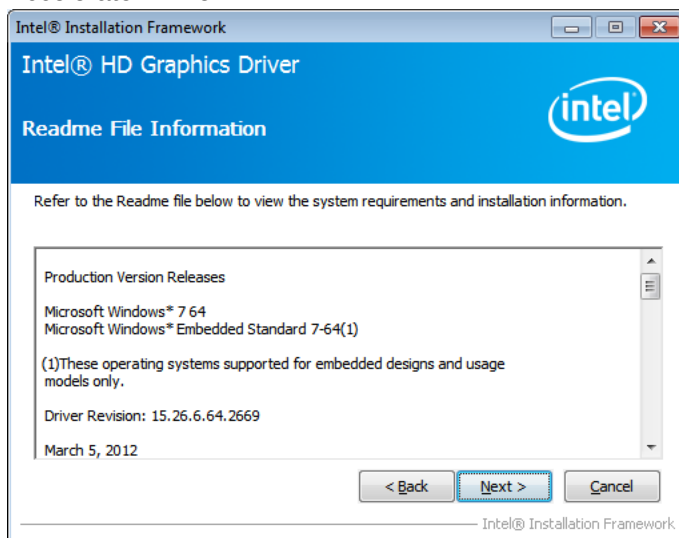
3. When the Welcome screen appears, click **Next** to continue.



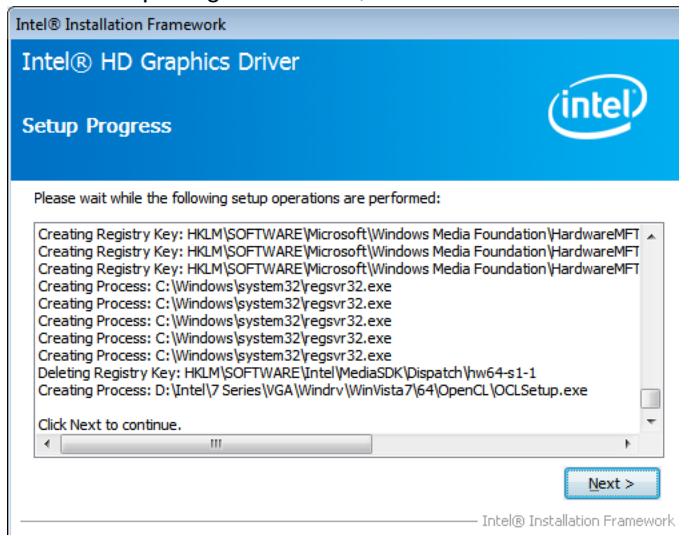
4. Click **Yes** to agree with the license agreement and continue the installation.



5. On the Readme File Information screen, click **Next** to continue the installation of the Intel® Graphics Media Accelerator Driver.



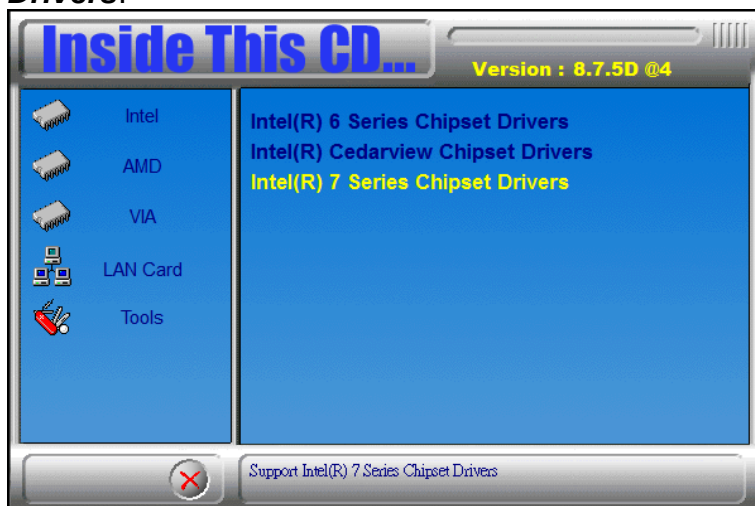
6. On Setup Progress screen, click **Next** to continue.



7. Setup complete. Click **Finish** to restart the computer and for changes to take effect.

LAN Drivers Installation

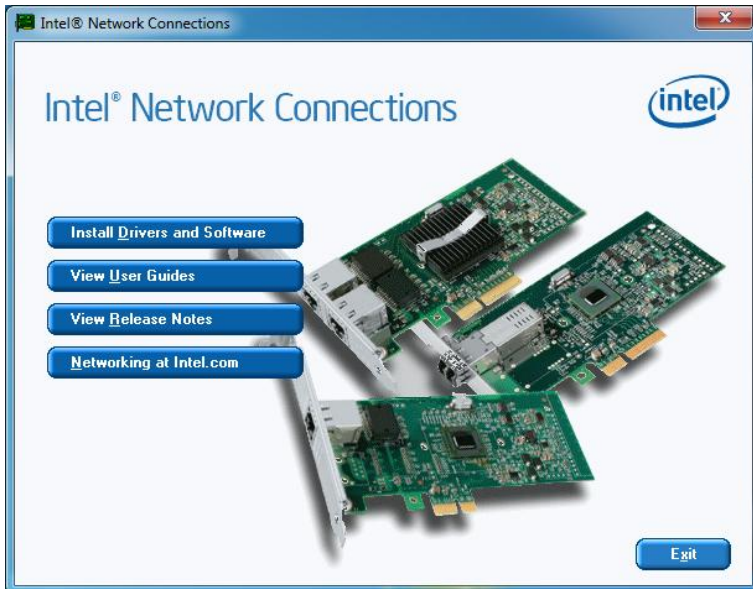
1. Insert the CD that comes with the board. Click **Intel** and then **Intel(R) Q7 Series Chipset Drivers**.



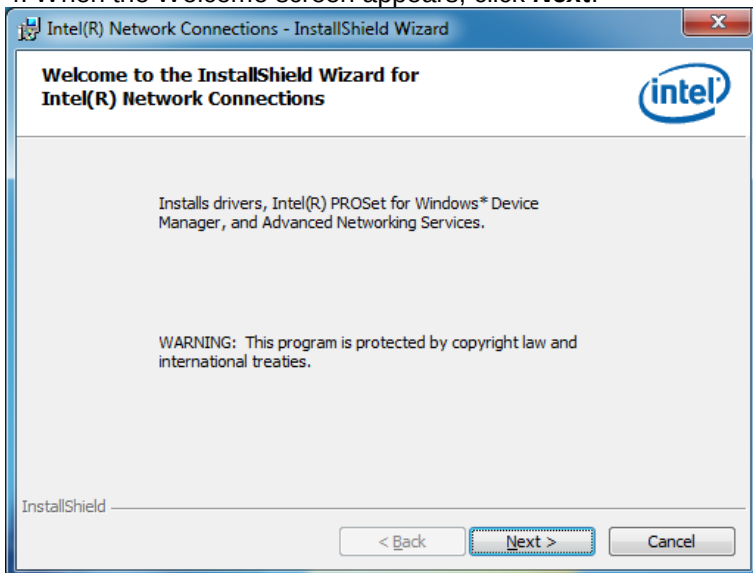
2. Click **Intel(R) PRO LAN Network Driver**.



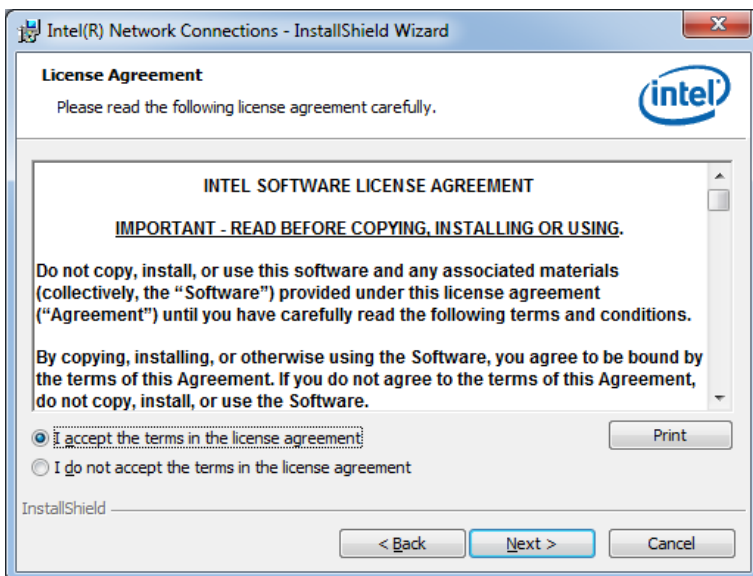
3. Click **Install Drivers and Software**.



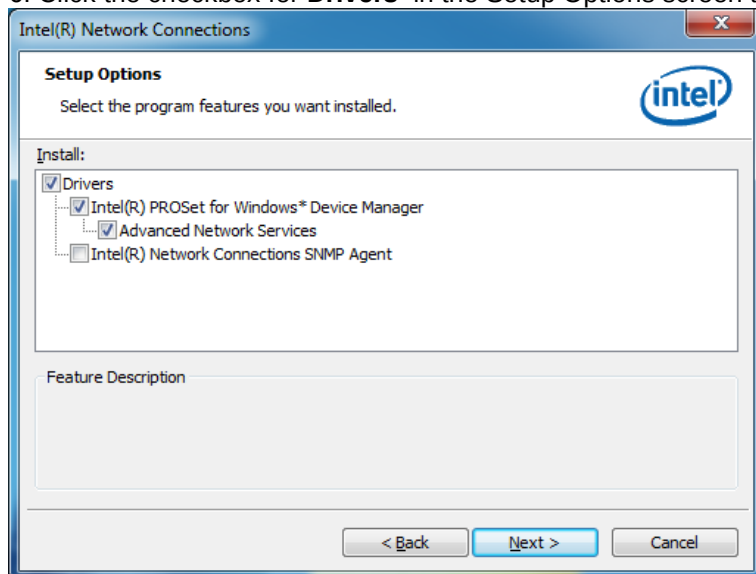
4. When the Welcome screen appears, click **Next**.



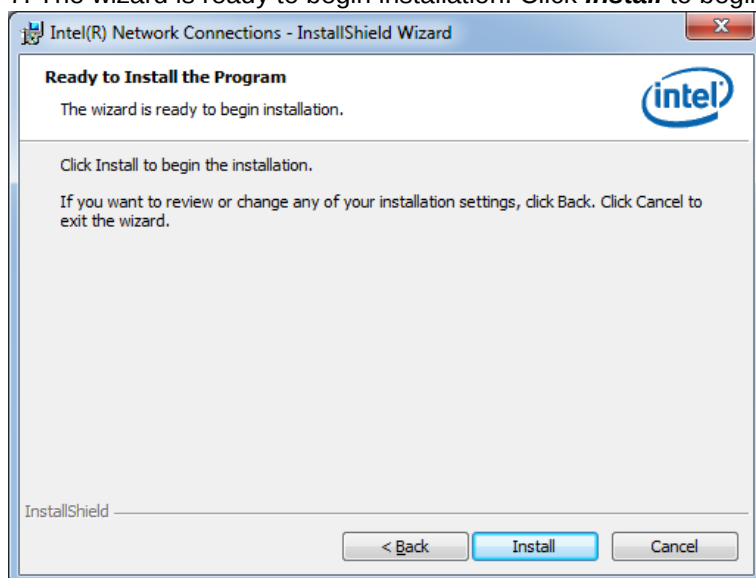
5. Click **Next** to to agree with the license agreement.



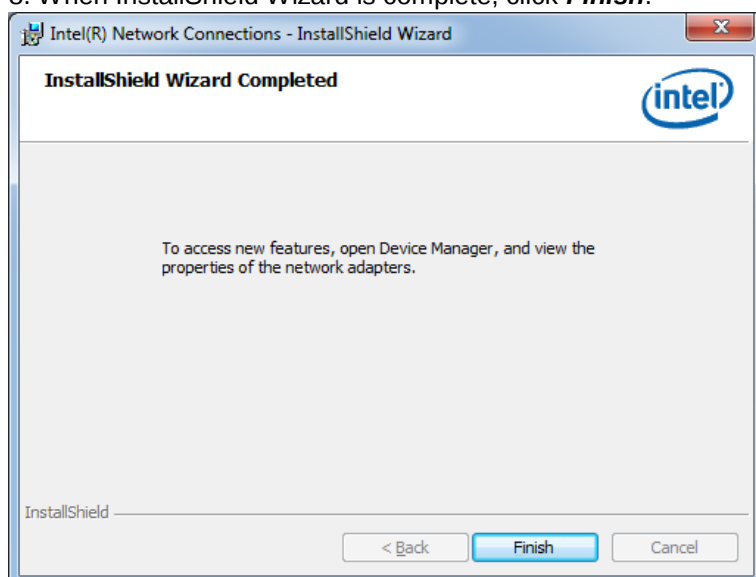
6. Click the checkbox for **Drivers** in the Setup Options screen to select it and click **Next** to continue.



7. The wizard is ready to begin installation. Click **Install** to begin the installation.



8. When InstallShield Wizard is complete, click **Finish**.



Intel® Management Engine Interface



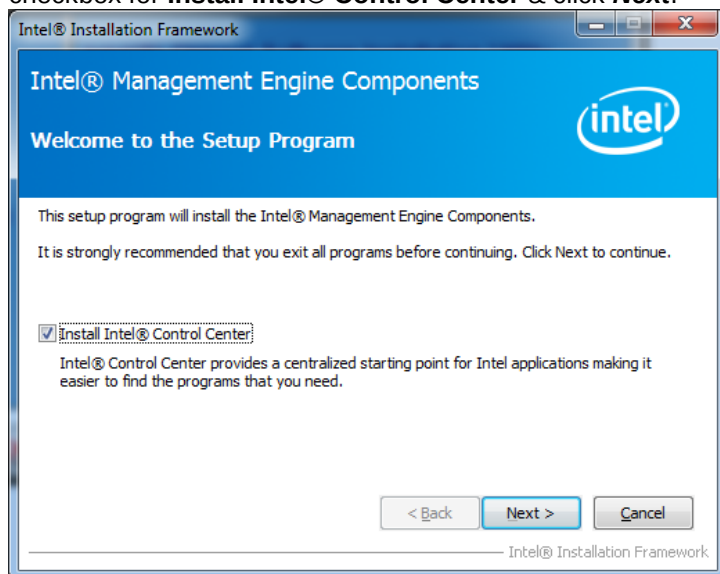
The following application requires Microsoft .NET Framework 3.5 or later: Intel® Management Engine Components. Please install the latest version of Microsoft .NET Framework from Microsoft Download Center to run this application correctly.

Follow the steps below to install the Intel Management Engine.

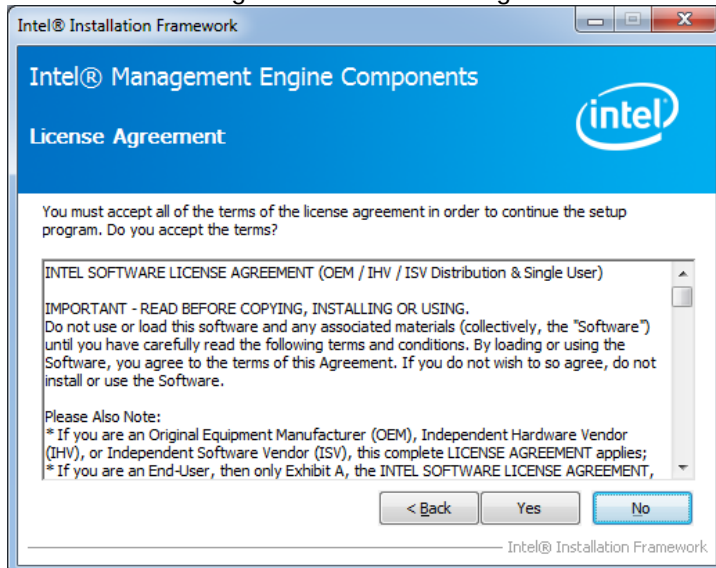
1. Insert the CD that comes with the board. Click **Intel** and then **Intel(R) AMT 8.0 Drivers**.



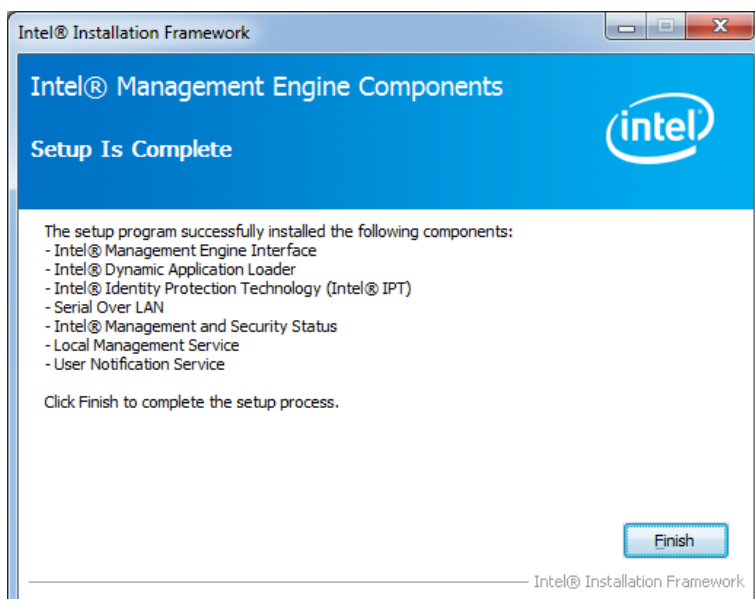
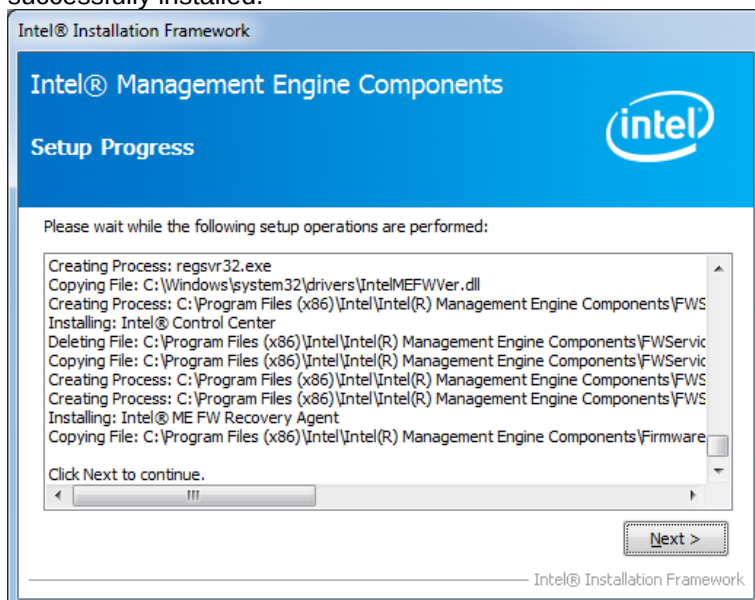
2. When the Welcome screen to the InstallShield Wizard for Intel® Management Engine Components, click the checkbox for **Install Intel® Control Center** & click **Next**.



3. Click **Yes** to agree with the license agreement.



4. When the Setup Progress screen appears, click **Next**. Then, click **Finish** when the setup progress has been successfully installed.



Intel® USB 3.0 Drivers

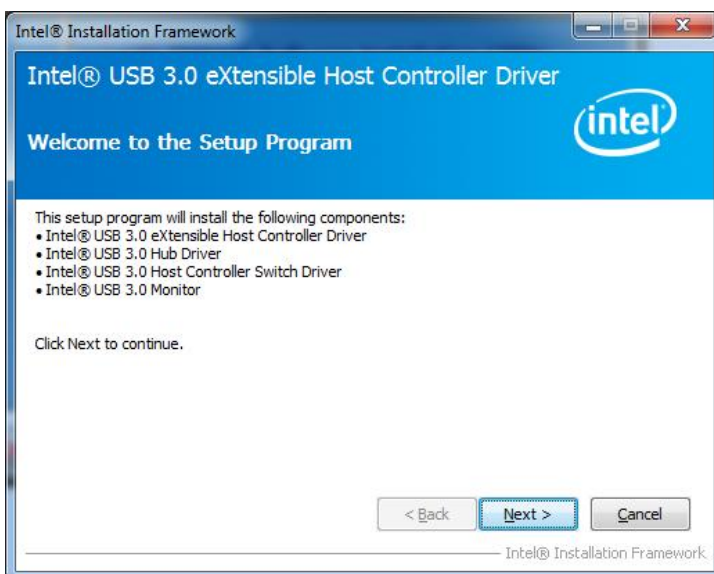
1. Insert the CD that comes with the board. Click **Intel** and then **Intel(R) C216 Series Chipset Drivers**.



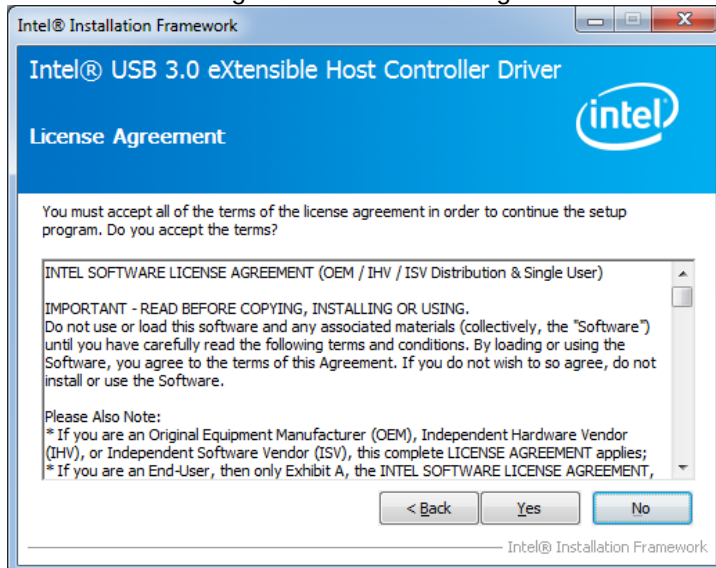
2. Click **Intel(R) USB 3.0 Drivers**.



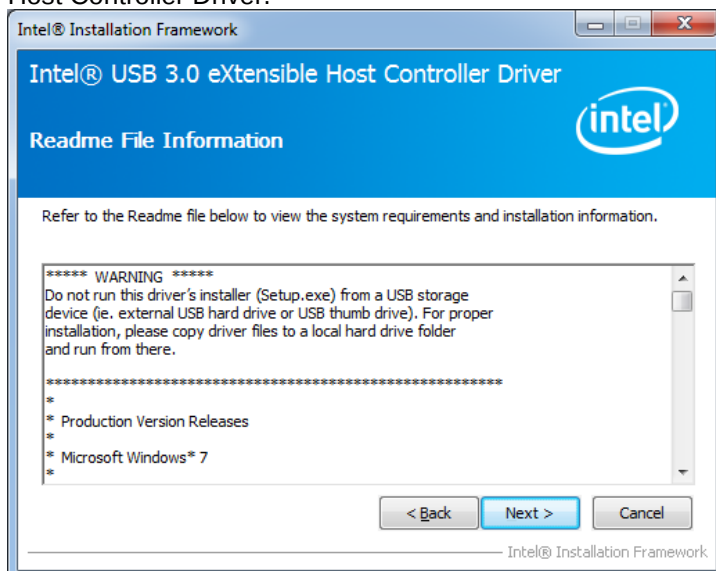
3. When the Welcome screen to the InstallShield Wizard for Intel® USB 3.0 eXtensible Host Controller Driver, click **Next**.



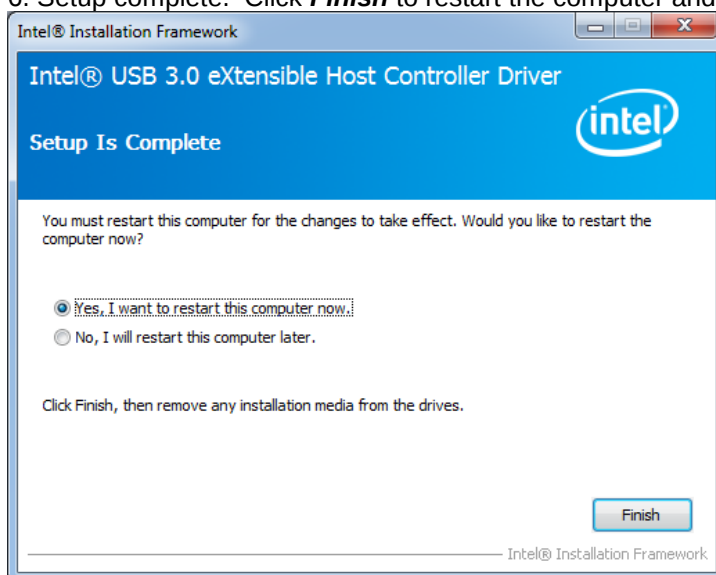
4. Click **Yes** to agree with the license agreement and continue the installation.



5. On the Readme File Information screen, click **Next** to continue the installation of the Intel® USB 3.0 eXtensible Host Controller Driver.



6. Setup complete. Click **Finish** to restart the computer and for changes to take effect.



Appendix-A I/O Port Address Map

Each peripheral device in the system is assigned a set of I/O port addresses which also becomes the identity of the device. The following table lists the I/O port addresses used.

Address	Device Description
000h - 01Fh	DMA Controller #1
020h - 03Fh	Interrupt Controller #1
040h - 05Fh	Timer
060h - 06Fh	Keyboard Controller
070h - 07Fh	Real Time Clock, NMI
080h - 09Fh	DMA Page Register
0A0h - 0BFh	Interrupt Controller #2
0C0h - 0DFh	DMA Controller #2
0F0h	Clear Math Coprocessor Busy Signal
0F1h	Reset Math Coprocessor
1F0h - 1F7h	IDE Interface
2F8h - 2FFh	Serial Port #2(COM2)
2B0h - 2DFh	Graphics adapter Controller
360h - 36Fh	Network Ports
3F8h - 3FFh	Serial Port #1(COM1)

Appendix-B Interrupt Request Lines (IRQ)

Peripheral devices use interrupt request lines to notify CPU for the service required. The following table shows the IRQ used by the devices on board.

Level	Function
IRQ0	System Timer Output
IRQ1	Keyboard
IRQ3	Serial Port #2
IRQ4	Serial Port #1
IRQ8	Real Time Clock
IRQ14	Primary IDE
IRQ15	Secondary IDE

Appendix-C FWA8308 Series Configurations

The following lists the available SKUs of FWA8308 for different system requirement.

FWA8308 2.5" HDD x1, PCI-e add-on card rear expansion x1, front panel expansion card x1, 300W PSU

- MB968 x1
- IP331 x1: 1-to-1 Riser Card
- IP332 x1: PCI-e Adapter
- Single 2.5" HDD Bracket x1
- 4-pin Smart Fan x3
- 300W Single Power Supply

FWA8308 Optional Items

- IBP161, IBP162...: Expansion LAN Card
- Dual 2.5" HDD Bracket Kit SC2FWA8308-0A1100P
- VGA cable: C501VGA0415272000P
- Console Cable: C501PK15108A12000P
- Rear Rackmount Kit: 600 or 800mm



FWA8308-2SLOT 3.5" HDD x1, PCI-e add-on card rear expansion x2, 300W PSU

- MB968 x1
- IP333 x1: 2-to-2 Riser Card
- Single 3.5" HDD Bracket x1
- 4-pin Smart Fan x3
- 300W Single Power Supply

FWA8308-2SLOT Optional Items

- Dual 2.5" HDD Bracket Kit SC2FWA8308-0A1100P
- VGA cable: C501VGA0415272000P
- Console Cable: C501PK15108A12000P
- Rear Rackmount Kit: 600 or 800mm



FWA8308-RPSU 2.5" HDD x1, PCI-e add-on card rear expansion x1, front panel expansion card x1, 275W 1+1 Redundant PSU

- MB968 x1
- IP331 x1: 1-to-1 Riser Card
- IP332 x1: PCI-e Adapter
- Single 2.5" HDD Bracket x1
- 4-pin Smart Fan x3
- 275W 1+1 Redundant Power Supply

FWA8308-RPSU Optional Items

- IBP161, IBP162...: Expansion LAN Card
- VGA cable: C501VGA0415272000P
- Console Cable: C501PK15108A12000P
- Rear Rackmount Kit: 600 or 800mm

