MI957

Intel ® Arrandale™ /PCH
Mini-ITX Motherboard

USER'S MANUAL

Version 1.0

Acknowledgments

Table of Contents

IMPORTANT NOTE: When the system boots without the CRT being connected, there will be no image on screen when you insert the CRT/VGA cable. To show the image on screen, the hotkey must be pressed (CTRL-ALT-F1).

Introduction

Product Description

The MI957 Mini ITX board incorporates the Intel® Chipset for Embedded Computing, consisting of the Intel® Arrandale DC mobile processor (integrated Graphic and Memory Controller) and Intel® Ibex Peak-M (PCH), an optimized integrated graphics solution with a 800/1066MHz front-side bus. Dimensions of the board are 170mm x 170mm.

The integrated graphics controller contains a refresh of the 5thgeneration graphics core support Intel® Dynamic Video Memory Technology, Smart 2D Display Technology, Clear Video Technology. It features a low-power design, is validated with the Intel® Arrandale DC mobile processors on 32nm process. With dual channel DDR3 800/1066MHz two w/ECC DIMM sockets on board, the board supports up to 8GB of DDR3 system memory.

The main features of the board are:

- Supports Intel® Arrandale DC mobile processor
- Supports up to 3.0GHz, 1066MHz FSB
- Two DDR3 w/ECC DIMM, Max. 8GB memory
- Onboard Gigabit MAC and PHY
- Integrated Graphics VGA for CRT /DVI/ LVDS
- 4x SATA, 12x USB 2.0, 4x COM, Watchdog timer
- 1x Mini PCI-E (Mini Card), 1x PCI, 1xPCI-E(x1) slots

Checklist

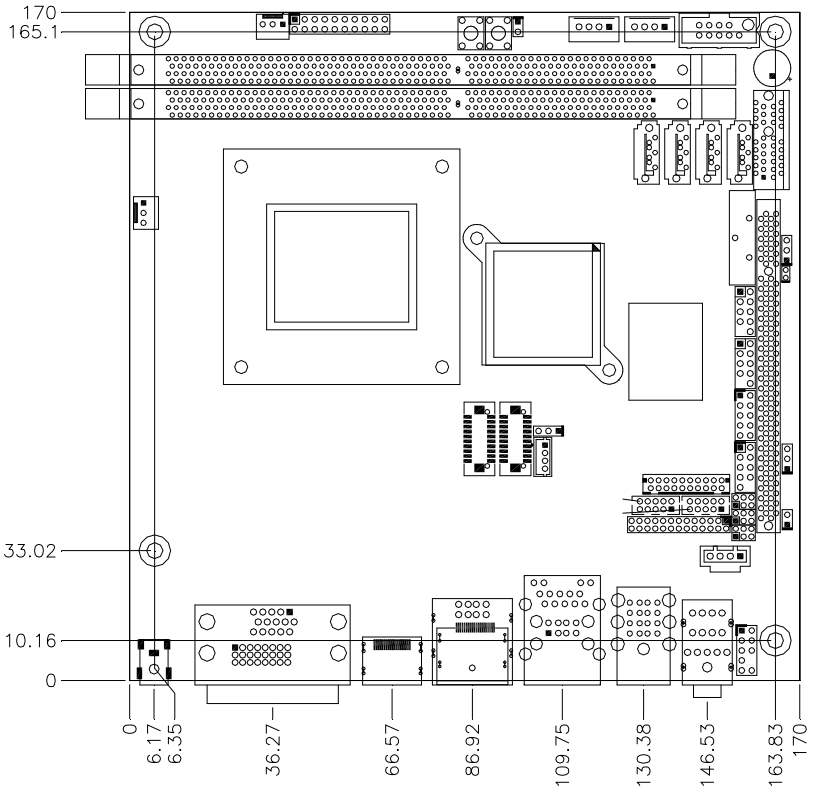
Your MI957 package should include the items listed below.

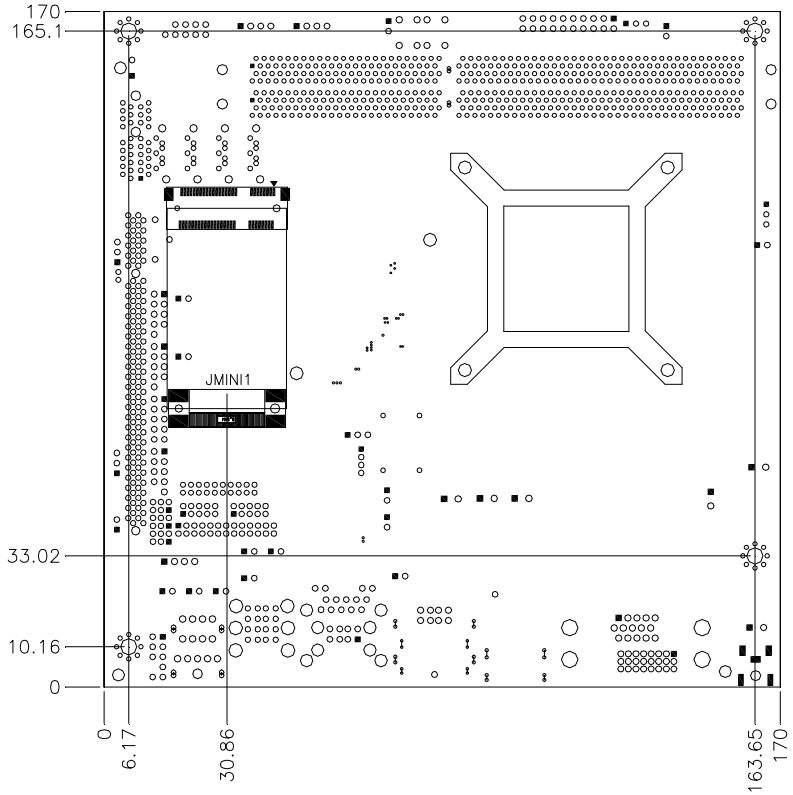
- The MI957 Mini-ITX motherboard
- This User's Manual
- 1 CD containing chipset drivers and flash memory utility
- Cable kit (Serial port, Serial ATA)

MI957 Specifications

CPU Supported	Intel® Arrandale+ECC processor - i7-610E (2.53GHz/4M Cache/ 2 cores/4 Threads/35W) - i3-330E (2.13GHz/3M Cache/ 2 cores/4 Threads/35W)
CPU Voltage	0.700V ~ 1.5V (IMVP-6.5)
System Speed	Up to 3.0GHz or above
CPU FSB	1066MHz FSB
Cache	Up to 4MB shared L3 Cache
Green /APM	APM1.2
CPU Tpye	FcBGA1288
Chipset	Intel Ibex Peak-M (PCH) Chipset PCH: 25mm x 27mm, 1071-pin FCBGA
BIOS	AMI BIOS, supports ACPI function
Memory	DDR3-800/1066 DIMM x2 (w/ECC function), Max. 8GB
VGA	Arrandale DC mobile processor integrated graphics Supports CRT, DVI Supports HDMI, DP(Display Port)
LVDS LCD Panel	Arrandale DC mobile processor built-in, supports 24-bit, single or dual channel LVDS
LAN	PCH 10/100/gigabit MAC + PHY • Intel 82577LM 10/100/1000
USB	PCH built-in USB 2.0 host controller, support 12 ports
Serial ATA Ports	PCH built-in SATA controller, supports 4 ports
IAMT6.0	PCH built-in Intel Active Management Technology VER 6.0 with HW KVM (MI957-i7-610E only)
Audio	PCH built-in High Definition audio controller:ALC888 w/ 5.1 channels
LPC I/O	F81865F: COM1, COM2 (RS232/RS422/RS485), COM3 and COM4 Hardware monitor (3 thermal, 4 voltage monitor inputs, 2 fan headers)
Digital IO	4 in & 4 out
Keyboard/Mouse	Supports PS/2 keyboard/mouse connector
Expansion Slots	PCI slot x1, PIC-E (x1) slot x1 and Mini PCIE socket x1
Edge Connector	PS/2 connector x1 for keyboard/mouse and dual USB stack connector Gigabit LAN RJ-45 + dual USB stack connector x1 DP Connect x1 + dual USB stack connector x1 HDMI connect x1 DVI-D and DB15 (VGA) stack connector x1 Quad USB stack connector x1 RCA Jack 3x1 for Audio (Front-Out, Line-In, Mic)
Onboard Header/ Connector	10-pin headerx1 for Digital I/O; 10-pin header x2 for COM1,COM2 20-pin header x1 for COM3, COM4 26-pin header x1 for Printer 10-pin header x 2 for USB 9,10,11,12 DF13 connector x2 for LVDS; 10-pin header x1 for audio Line-Out & Mic 4-pin header x1 for CD in, SPDIF-out connector x1 SATA connector x4 for SATA ports
Watchdog Timer	Yes (256 segments, 0, 1, 2…255 sec/min)
System Voltage	+5V, +3.3V, +12V, -12V, 5VSB
Others	Modem Wakeup, LAN Wakeup
Board Size	170mm x 170mm (Mini ITX)

Board Dimensions

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165.1
JMINI1
33.02
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6.17
30.86
163.65
170

Installations

This section provides information on how to use the jumpers and connectors on the MI957 in order to set up a workable system. The topics covered are:

Installing the CPU

The MI957 board supports FcBGA1288 for Intel® Arrandale Dual Core mobile processors.

***NOTE**: Ensure that the CPU heat sink and the CPU top surface are in total contact to avoid CPU overheating problem that would cause your system to hang or be unstable.*

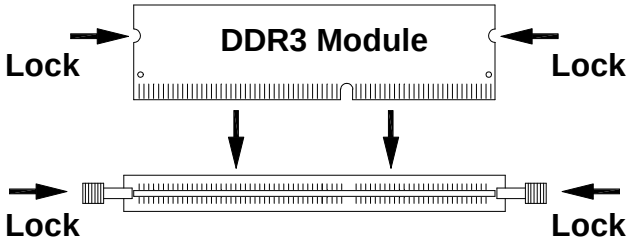
Installing the Memory

The MI957 board supports two DDR3 memory socket for a maximum total memory of 8GB in DDR3 w/ECC DIMM memory type.

Installing and Removing Memory Modules

To install the DDR3 modules, locate the memory slot on the board and perform the following steps:

1. Hold the DDR3 module so that the key of the DDR3 module aligned with that on the memory slot.
2. Gently push the DDR3 module in an upright position until the clips of the slot close to hold the DDR3 module in place when the DDR3 module touches the bottom of the slot.
3. To remove the DDR3 module, press the clips with both hands.

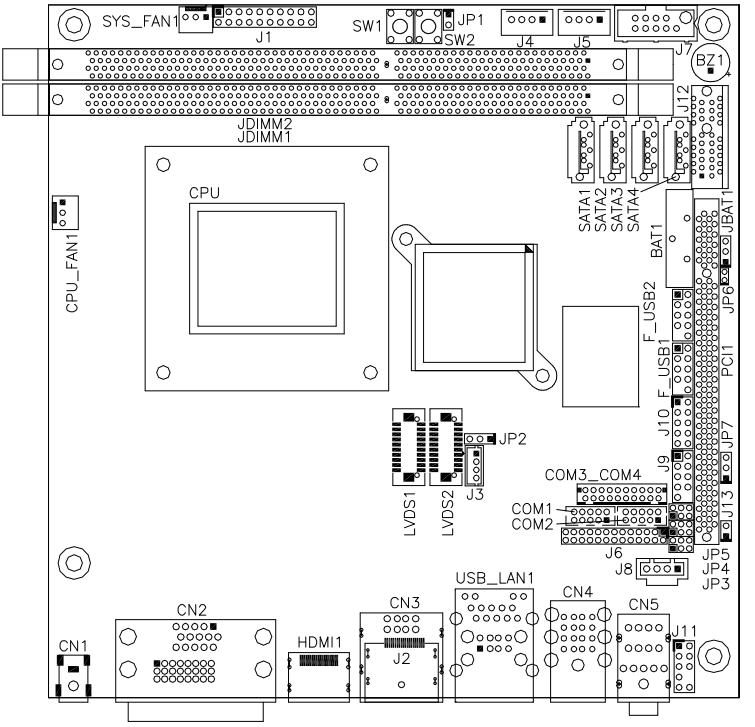


Setting the Jumpers

Jumpers are used on MI957 to select various settings and features according to your needs and applications. Contact your supplier if you have doubts about the best configuration for your needs. The following lists the connectors on MI957 and their respective functions.

IMPORTANT NOTE: When the system boots without the CRT being connected, there will be no image on screen when you insert the CRT/VGA cable. To show the image on screen, the hotkey must be pressed.

Jumper Locations on MI957

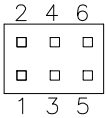


JP2: LCD Panel Power Selection

JP1	LCD Panel Power
	3.3V
	5V

JP3, JP4, JP5: RS232/422/485 (COM2) Selection

COM1 is fixed for RS-232 use only.
COM2 is selectable for RS232, RS-422 and RS-485.
The following table describes the jumper settings for COM2 selection.



COM2 Function	RS-232	RS-422	RS-485
Jumper Setting (pin closed)	JP3: 1-2 JP4: 3-5 & 4-6 JP5: 3-5 & 4-6	JP3: 3-4 JP4: 1-3 & 2-4 JP5: 1-3 & 2-4	JP3: 5-6 JP4: 1-3 & 2-4 JP5: 1-3 & 2-4

COM2 is jumper selectable for RS-232, RS-422 and RS-485.

Pin #	Signal Name		
	RS-232	**R2-422**	**RS-485**
1	DCD	TX-	DATA-
2	RX	TX+	DATA+
3	TX	RX+	NC
4	DTR	RX-	NC
5	Ground	Ground	Ground
6	DSR	RTS-	NC
7	RTS	RTS+	NC
8	CTS	CTS+	NC
9	RI	CTS-	NC
10	NC	NC	NC

JP7: PCI/PCIE Riser Card Selection

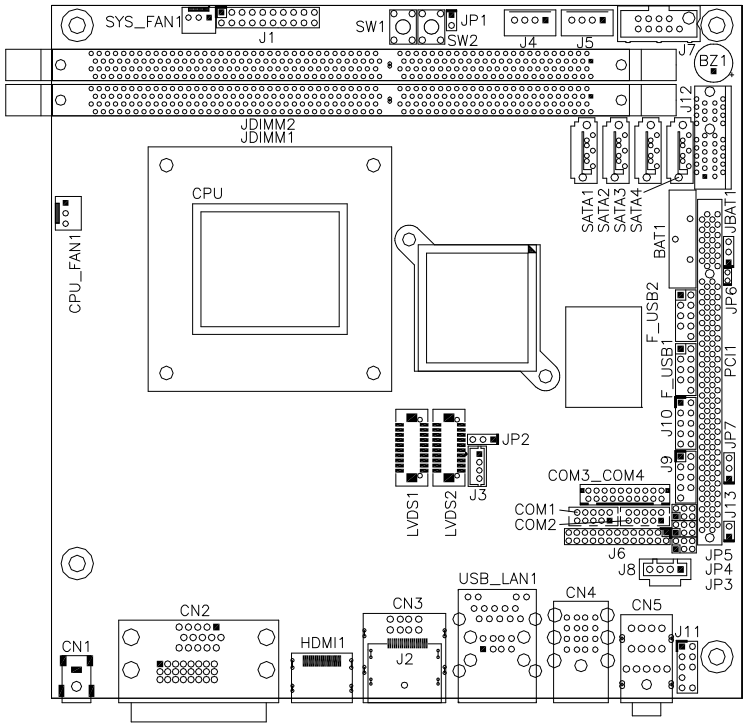
JP6	Riser Card
	IP390 Riser Card Install
	IP151, IP240 Riser Card Install

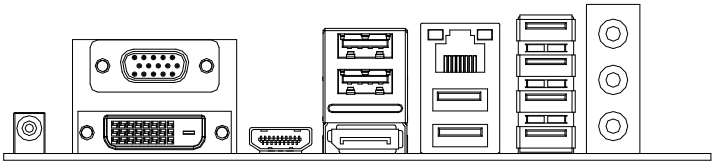
JBAT1: Clear CMOS Setting

JBAT1	Setting
	Normal
	Clear CMOS

Connectors on MI957

Connector Locations on MI957

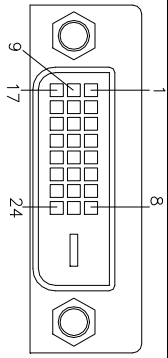




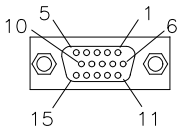
CN1: DC Adapter Connector

CN1 provides DC12V that provide system power +5,+3.3,+12V,5VSB

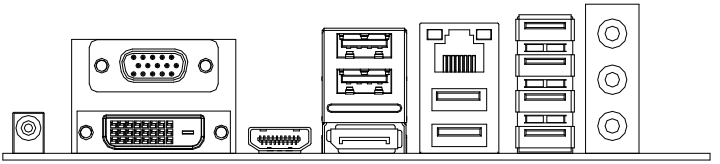
CN2: DVI-D and VGA Connector



Signal Name	Pin #	Pin #	Signal Name
DATA 2-	**1**	**16**	**HOT PLUG**
DATA 2+	2	17	DATA 0-
Shield 2/4	3	18	DATA 0+
DATA 4-	4	19	SHIELD 0/5
DATA 4+	5	20	DATA 5-
DDC CLOCK	6	21	DATA 5+
DDC DATA	7	22	SHIELD CLK
N.C	8	23	CLOCK -
DATA 1-	9	24	CLOCK +
DATA 1+	10	C1	N.C.
SHIELD 1/3	11	C2	N.C.
DATA 3-	12	C3	N.C.
DATA 3+	13	C4	N.C.
DDC POWER	14	C5	N.C.
A GROUND 1	15	C6	N.C.



Signal Name	Pin #	Pin #	Signal Name
Red	1	2	Green
Blue	3	4	N.C.
GND	5	6	GND
GND	7	8	GND
N.C.	9	10	GND
N.C.	11	12	DDC_DATA
HSYNC	13	14	VSYNC
DDC_CLK	15		



HDMI1: HDMI Connector

Signal Name	Pin #	Pin #	Signal Name
DATA 2-	**1**	**13**	**DATA 3+**
DATA 2+	2	14	+5V Power
Shield 2/4	3	15	GROUND
DATA 4-	4	16	**HOT PLUG**
DATA 4+	5	17	DATA 0-
DDC CLOCK	6	18	DATA 0+
DDC DATA	7	19	SHIELD 0/5
N.C	8	20	DATA 5-
DATA 1-	9	21	DATA 5+
DATA 1+	10	22	SHIELD CLK
SHIELD 1/3	11	23	CLOCK +
DATA 3-	12	24	CLOCK -

CN3: USB11/12 Ports

J2: Display Port Connector

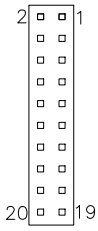
CN4: USB6/7/8/10 Ports

USB_LAN1: 10/100/1000 RJ-45 and USB9/13 Ports

CN5: Audio Connector

The audio connector, from top to bottom, is composed of Line in, Line out and Microphone jacks.

COM3_COM4: COM3, COM4 Serial Port



Signal Name	Pin #	Pin #	Signal Name
DSR	2	1	DCD
RTS	4	3	RXD
CTS	6	5	TXD
RI	8	7	DTR
NA	10	9	Ground
DSR	12	11	DCD
RTS	14	13	RXD
CTS	16	15	TXD
RI	18	17	DTR
NA	20	19	Ground

SYS_FAN1: System Fan Power Connector

This is a 3-pin header for system fans. The fan must be a 12V (500mA).

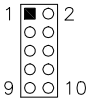
Pin #	Signal Name
1	Ground
2	+12V
3	Rotation detection

CPU_FAN1: CPU Fan Power Connector

This is a 3-pin header for the CPU fan. The fan must be a 12V fan.

Pin #	Signal Name
1	Ground
2	+12V
3	Rotation detection

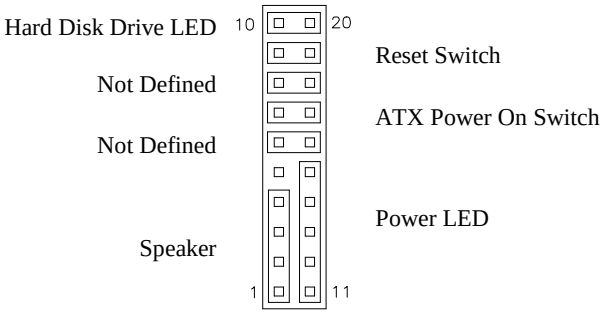
J9: PS/2 Keyboard/Mouse Connector



Signal Name	Pin	Pin	Signal Name
Ground	1	2	Ground
Vcc	3	4	Vcc
MSDATA	5	6	KBDATA
MSCLK	7	8	KBCLK
NC	9	10	NC

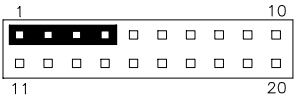
J1 (F_PANEL): System Function Connector

J1 provides connectors for system indicators that provide light indication of the computer activities and switches to change the computer status. J2 is a 20-pin header that provides interfaces for the following functions.



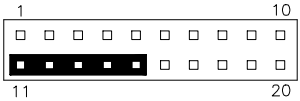
Speaker: Pins 1 - 4

This connector provides an interface to a speaker for audio tone generation. An 8-ohm speaker is recommended.



Pin #	Signal Name
1	Speaker out
2	No connect
3	Ground
4	+5V

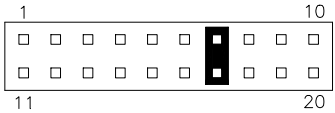
Power LED: Pins 11 - 15



Pin #	Signal Name
11	Power LED
12	No connect
13	Ground
14	No connect
15	Ground

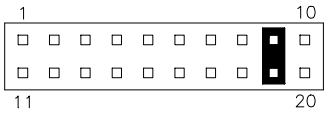
ATX Power ON Switch: Pins 7 and 17

This 2-pin connector is an "ATX Power Supply On/Off Switch" on the system that connects to the power switch on the case. When pressed, the power switch will force the system to power on. When pressed again, it will force the system to power off.



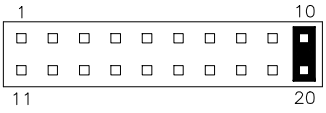
Reset Switch: Pins 9 and 19

The reset switch allows the user to reset the system without turning the main power switch off and then on again. Orientation is not required when making a connection to this header.



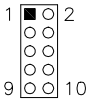
Hard Disk Drive LED Connector: Pins 10 and 20

This connector connects to the hard drive activity LED on control panel. This LED will flash when the HDD is being accessed.



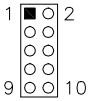
Pin #	Signal Name
10	HDD Active
20	5V

F_USB1: USB1/USB5 Connector



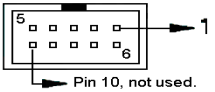
Signal Name	Pin	Pin	Signal Name
Vcc	1	2	Vcc
D0-	3	4	D1-
D0+	5	6	D1+
Ground	7	8	Ground
NC	9	10	Ground

F_USB2: USB0/USB3 Connector



Signal Name	Pin	Pin	Signal Name
Vcc	1	2	Vcc
D0-	3	4	D1-
D0+	5	6	D1+
Ground	7	8	Ground
NC	9	10	Ground

COM1,COM2: COM1,COM2 Serial Port

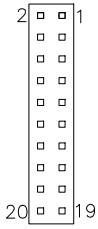


COM2

Signal Name	Pin #	Pin #	Signal Name
DCD, Data carrier detect	1	6	DSR, Data set ready
RXD, Receive data	2	7	RTS, Request to send
TXD, Transmit data	3	8	CTS, Clear to send
DTR, Data terminal ready	4	9	RI, Ring indicator
GND, ground	5	10	Not Used

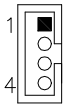
LVDS1, LVDS2: LVDS Connectors (1st channel, 2nd channel)

The LVDS connectors on board consist of the first channel (LVDS1) and second channel (LVDS2).



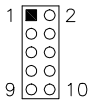
Signal Name	Pin #	Pin #	Signal Name
TX0-	2	1	TX0+
Ground	4	3	Ground
TX1-	6	5	TX1+
5V/3.3V	8	7	Ground
TX3-	10	9	TX3+
TX2-	12	11	TX2+
Ground	14	13	Ground
TXC-	16	15	TXC+
5V/3.3V	18	17	ENABKL
+12V	20	19	+12V

J3: LCD Backlight Connector



Pin #	Signal Name
1	+12V
2	Backlight Enable
3	Brightness Control
4	Ground

J10: Digital I/O



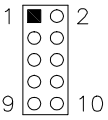
Signal Name	Pin	Pin	Signal Name
GND	1	2	VCC
OUT3	3	4	OUT1
OUT2	5	6	OUT0
IN3	7	8	IN1
IN2	9	10	IN0

J8: CD-In Pin Header

Pin #	Signal Name
1	CD Audio R
2	Ground
3	Ground
4	CD Audio L

J7: SPI Flash Connector (factory use only)

J11: Front Audio Connector



Signal Name	Pin #	Pin #	Signal Name
MIC2_L	1	2	Ground
MIC2_R	3	4	Presence#
Line2_L	5	6	MIC2_ID
Sense	7	8	NC
Line2_R	9	10	Line2_ID

J12: PCI-E(x1) Slot

J13: SPDIF Out Connector

PCI1: PCI Slot (supports 2 Master)

JMINI: Mini PCIE Connector

SATA1, SATA2, SATA3, SATA4: SATA Connectors

J4, J5: +12V and +5V Output Power Connectors

J6: Printer Port Connectors

BIOS Setup

This chapter describes the different settings available in the AMI BIOS that comes with the board. The topics covered in this chapter are as follows:

BIOS Introduction

The BIOS (Basic Input/Output System) installed in your computer system's ROM supports Intel processors. The BIOS provides critical low-level support for a standard device such as disk drives, serial ports and parallel ports. It also password protection as well as special support for detailed fine-tuning of the chipset controlling the entire system.

BIOS Setup

The BIOS provides a Setup utility program for specifying the system configurations and settings. The BIOS ROM of the system stores the Setup utility. When you turn on the computer, the BIOS is immediately activated. Pressing the <Del> key immediately allows you to enter the Setup utility. If you are a little bit late pressing the <Del> key, POST (Power On Self Test) will continue with its test routines, thus preventing you from invoking the Setup. If you still wish to enter Setup, restart the system by pressing the "Reset" button or simultaneously pressing the <Ctrl>, <Alt> and <Delete> keys. You can also restart by turning the system Off and back On again. The following message will appear on the screen:

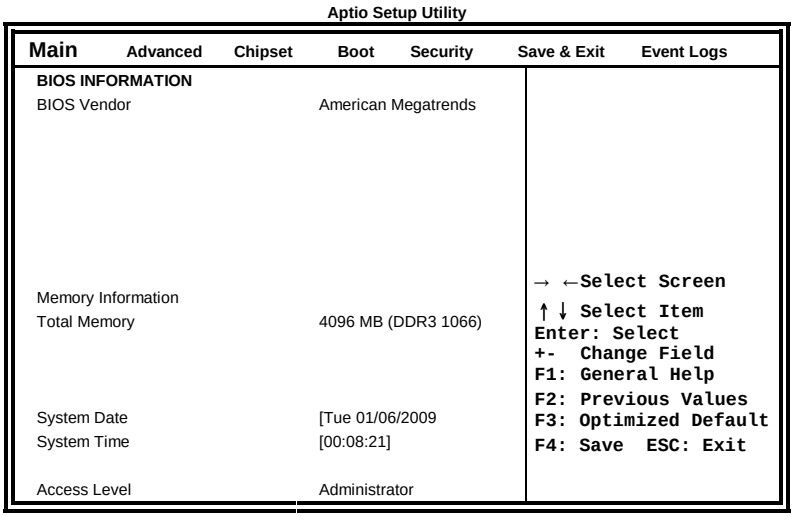
```
Press  <DEL>  to  Enter  Setup
```

In general, you press the arrow keys to highlight items, <Enter> to select, the <PgUp> and <PgDn> keys to change entries, <F1> for help and <Esc> to quit.

When you enter the Setup utility, the Main Menu screen will appear on the screen. The Main Menu allows you to select from various setup functions and exit choices.

Main BIOS Setup

This setup allows you to record some basic hardware configurations in your computer system and set the system clock.



***Note**: If the system cannot boot after making and saving system changes with Setup, the AMI BIOS supports an override to the CMOS settings that resets your system to its default.*

***Warning:** It is strongly recommended that you avoid making any changes to the chipset defaults. These defaults have been carefully chosen by both AMI and your system manufacturer to provide the absolute maximum performance and reliability. Changing the defaults could cause the system to become unstable and crash in some cases.*

System Language

Choose the system default language.

System Date

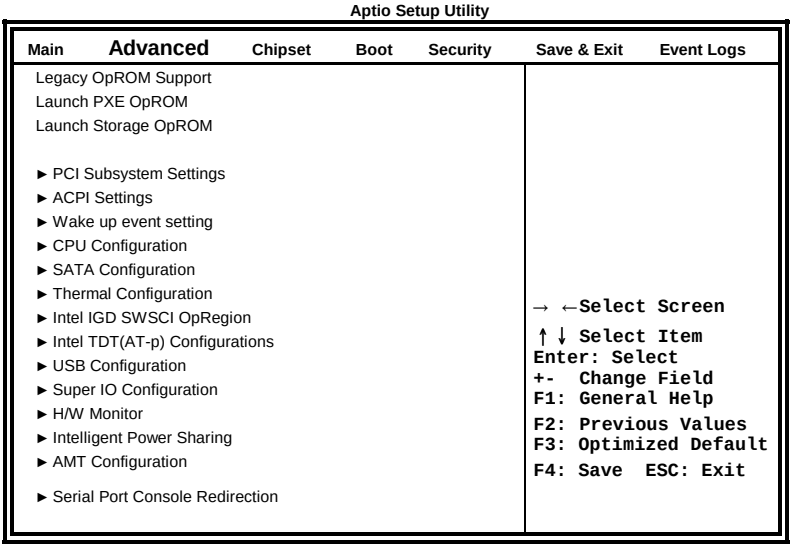
Set the Date. Use Tab to switch between Data elements.

System Time

Set the Time. Use Tab to switch between Data elements.

Advanced Settings

This section allows you to configure and improve your system and allows you to set up some system features according to your preference.



Launch PXE OpROM

Enable or Disable Boot Option for Legacy Network Devices.

Launch Storage OpROM

Enable or Disable Boot Option for Legacy Mass Storage Devices with Option ROM.

► Wake up event setting

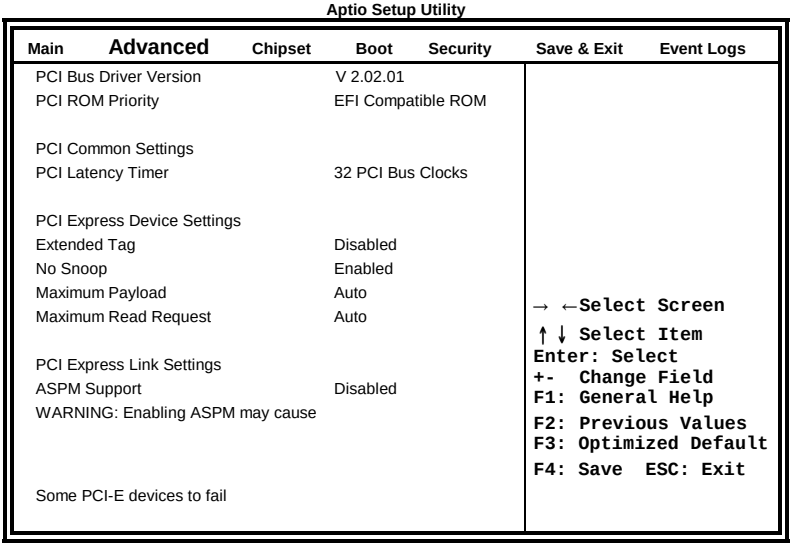
Enable/Disable Wake up event.

► Intel TDT(AT-p) Configurations

Disabling TDT Allow user to login to platform. This is strictly for testing only. This does not disable TDT Services in ME.

PCI Subsystem Settings

This section allows you to configure the PCI, PCI-X and PCI Express settings.



PCI ROM Priority

In case of multiple Option ROMs (Legacy and EFI Compatible), specifies what PCI Option ROM to launch.

PCI Latency Timer

Value to be programmed into PCI Latency Timer Register.

Extended Tag

If ENABLED allows Device to use 8-bit Tag field as a requester.

No Snoop

Enables or Disables PCI Express Device No Snoop option.

Maximum Payload

Set Maximum Payload of PCI Express Device or allow System BIOS to select the value.

Maximum Read Request

Launches (Enabled/Disabled) the boot option for legacy network devices.

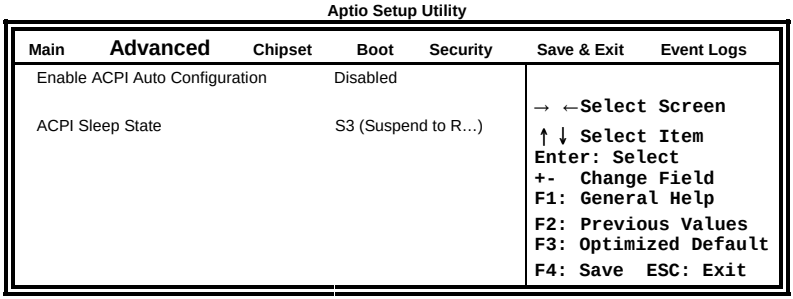
PCI Express Link Settings

Set Maximum Read Request Size of PCI Express Device or allow System BIOS to select the value.

ASPM Support

Set the ASPM Level:
Force L0 – Force all links to L0 State
AUTO – BIOS auto configure
DISABLE – Disables ASPM

ACPI Settings



Enabled ACPI Auto Configuration

Enables or Disables BIOS ACPI Auto Configuration.

ACPI Sleep State

Select the highest ACPI sleep state the system will enter, when the SUSPEND button is pressed.

Wake up event settings

Aptio Setup Utility

Main	Advanced	Chipset	Boot	Security	Save & Exit	Event Logs
Wake system with Fixed Time			Disabled			
Wake up hour			0		→ ←Select Screen	
Wake up minute			0		↑ ↓ Select Item	
Wake up second			0		Enter: Select	
					+- Change Field	
Wake on Ring			Disabled		F1: General Help	
Wake on PCI PME			Disabled		F2: Previous Values	
Wake on PCIE Wake Event			Disabled		F3: Optimized Default	
					F4: Save ESC: Exit	

Wake system with Fixed Time

Enables or Disables System wake on alarm event. When enabled, System will wake on the hr::min:: sec specified.

Wake on Ring

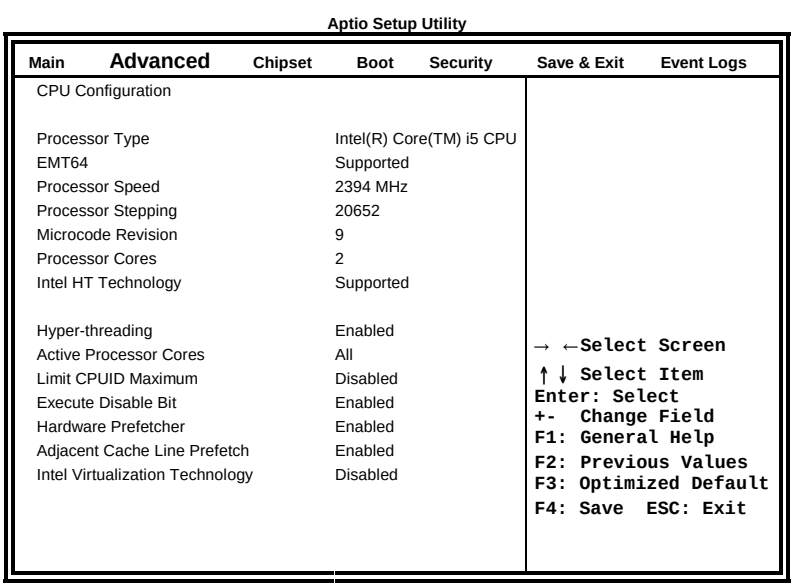
The options are Disabled and Enabled.

Wake on PCI PME

The options are Disabled and Enabled.

CPU Configuration

This section shows the CPU configuration parameters.



Hyper-threading

Enabled for Windows XP and Linux (OS optimized for Hyper-Threading Technology) and Disabled for other OS (OS not optimized for Hyper-Threading Technology). When Disabled, only one thread per enabled core is enabled.

Active Processor Cores

Number of cores to enable in each processor package.

Limit CPUID Maximum

Disabled for Windows XP.

Execute Disable Bit

XD can prevent certain classes of malicious buffer overflow attacks when combined with a supporting OS (Windows Server 2003 SP1, Windows XP SP2, SuSE Linux 9.2, Re33dHat Enterprise 3 Update 3.)

Hardware Prefetcher

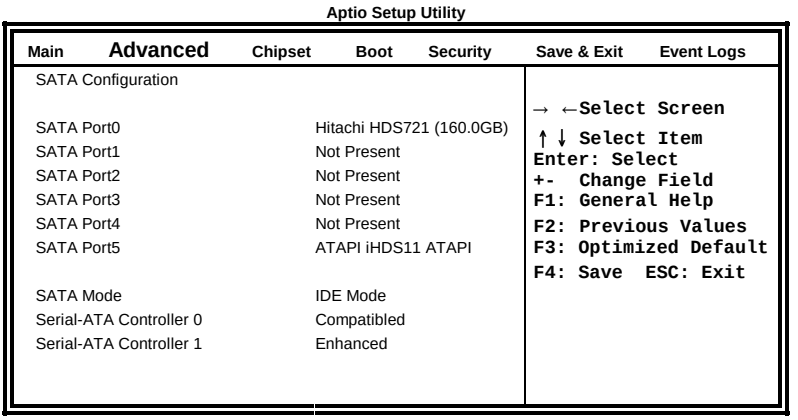
To turn on/off the MLC streamer prefetcher.

Adjacent Cache Line Prefetch
To turn on/off prefetching of adjacent cache lines.

Intel Virtualization Technology
When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology.

Power Technology
Enable the power management features.

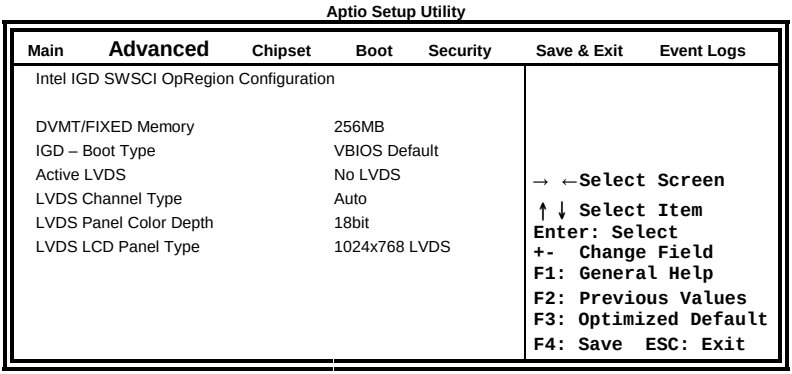
SATA Configuration
SATA Devices Configuration.



SATA Mode
Options are:
(1) IDE Mode
(2) AHCI Mode
(3) RAID Mode

Serial-ATA Controller
Options are:
Disable
(1) Enhanced
(2) Compatible

Intel IGD SWSCI OpRegion



DVMT/FIXED Memory

Select DVMT/FIXED Mode Memory size used by Internal Graphics Device. Options are 128MB, 256MB and Maximum.

IGD – Boot Type

Select the Video Device which will be activated during POST. This has no effect if external graphics present. Options are VBIOS Default, CRT, LVDS, Display Port, HDMI, DVI, CRT+LVDS, CRT+HDMI and CRT+DVI.

Active LVDS

Select the Active LVDS Configuration.
No LVDS: VBIOS does not enable LVDS.
Int-LVDS: VBIOS enables LVDS driver by Integrated encoder.
SDVO LVDS : VBIOS enables LVDS driver by SDVO encoder.
eDP: LVDS Driven by Int-DisplayPort encoder.

LVDS Channel Type

The default setting is Auto. Other settings are Single and Double.

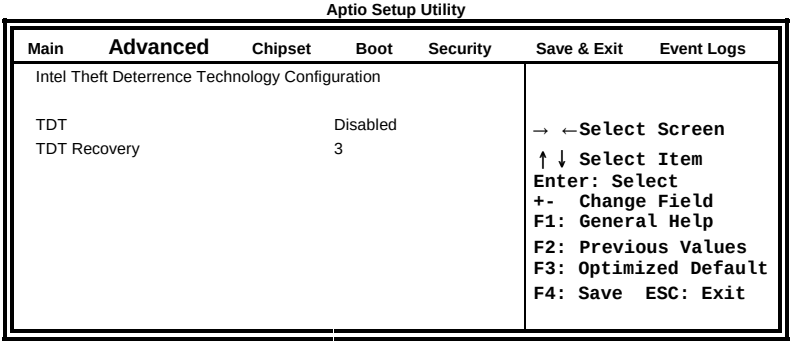
LVDS Panel Color Depth

The default setting is 18bit. The other optoin is 24bit.

LVDS LCD Panel Type

The default setting is 1024x768 LVDS.

Intel TDT(AT-p) Configurations



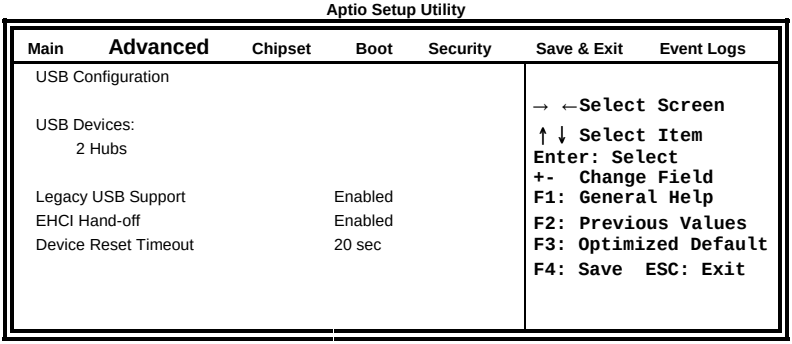
TDT

Enable/Disable TDT in BIOS for testing only.

TDT Recovery

Set the number of times Recovery attempted will be allowed.

USB Configuration



Legacy USB Support

Enables Legacy USB support.
AUTO option disables legacy support if no USB devices are connected.
DISABLE option will keep USB devices available only for EFI applications.

EHCI Hand-off

Enabled/Disabled. This is a workaround for Oses without EHCI hand-off support. The EHCI ownership change should be claimed by EHCI driver.

Device Reset Timeout

USB mass storage device Start Unit command timeout.
Options are: 10 sec / 20 sec / 30 sec / 40 sec.

Super IO Configuration

Aptio Setup Utility

Main	Advanced	Chipset	Boot	Security	Save & Exit	Event Logs
Super IO Configuration						
Super IO Chip			Fintek F81865			
-> Serial Port 0 Configuration						
-> Serial Port 1 Configuration						
-> Serial Port 2 Configuration						
-> Serial Port 3 Configuration						
Parallel Port Configuration						
Power Failure			Always off			
ACPI Shutdown Temperature			Disable			

→ ←Select Screen
↑ ↓ Select Item
Enter: Select
+- Change Field
F1: General Help
F2: Previous Values
F3: Optimized Default
F4: Save ESC: Exit

Serial Port Configuration

Set Parameters of Serial Ports. User can Enable/Disable the serial port and Select an optimal settings for the Super IO Device.

Power Failure

Options are:
Keep last state
Bypass mode
Always on
Always off (default)

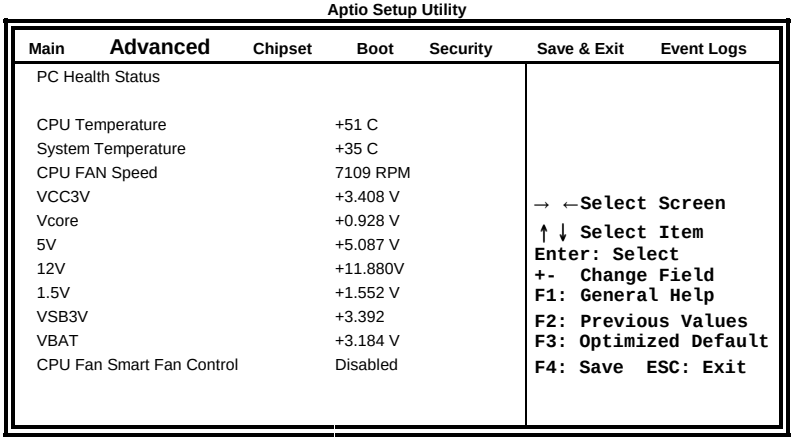
Parallel Port Configuration

Set Parameters of the parallel port. The default setting is 378F/IRQ7.

ACPI Shutdown Temperature

The system will shut down automatically under OS with ACPI mode, when the CPU temperature reaches the configured temperature.

H/W Monitor



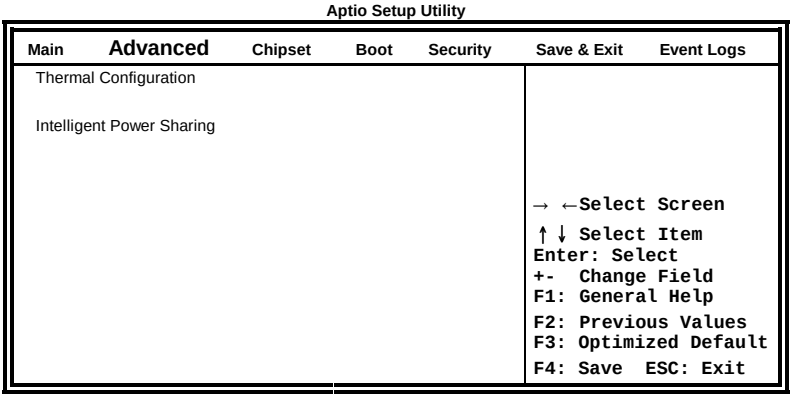
Temperatures/Voltages

These fields are the parameters of the hardware monitoring function feature of the motherboard. The values are read-only values as monitored by the system and show the PC health status.

CPU Fan Smart Fan Control

This field enables or disables the smart fan feature. At a certain temperature, the fan starts turning. Once the temperature drops to a certain level, it stops turning again.

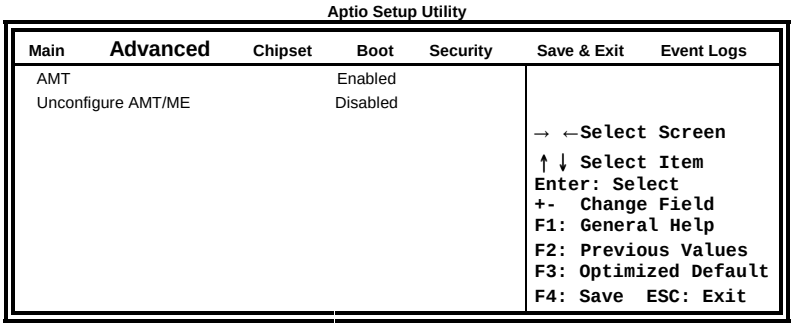
Thermal Configuration



Intelligent Power Sharing

- Intelligent power sharing – The default setting is Enabled.
- Mch Turbo – The default setting is Enabled.
- IPS Policy – The default setting is Driver.
- Core Temp Limit – The default setting is Disabled.
- Mch Power Limit – The default setting is Disabled.
- Processor Power Limit - The default setting is Disabled.
- Core Power Limit – The default setting is Disabled.

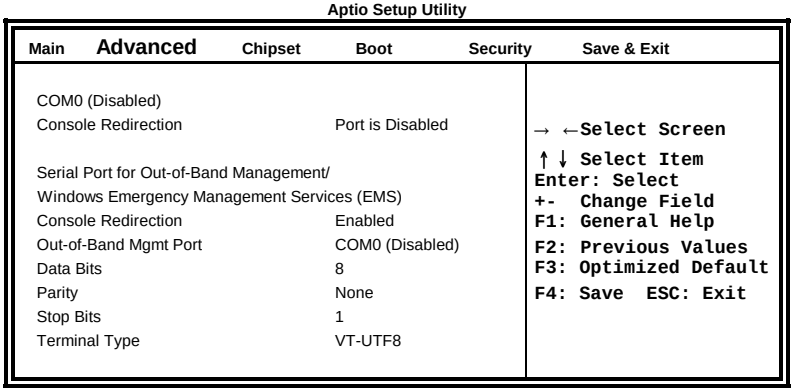
AMT Configuration



AMT
Options are Enabled and Disabled.

Unconfigure AMT/ME
Perform AMT/ME unconfigure without password operation.

Serial Port Console Redirection

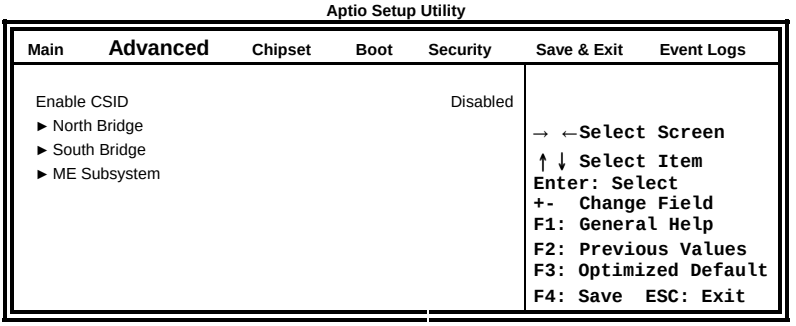


Console Redirection
Console Redirection Enable/Disable.

Terminal Type
VT-UTF8 is the preferred terminal type for out-of-band management. The next best choice is VT100+ and then VT100.

Chipset Settings

This section allows you to configure and improve your system and allows you to set up some system features according to your preference.



Enable CSID

By default, this item is disabled. Enable Compatible Revision ID.

North Bridge

This item shows the North Bridge Parameters.

South Bridge

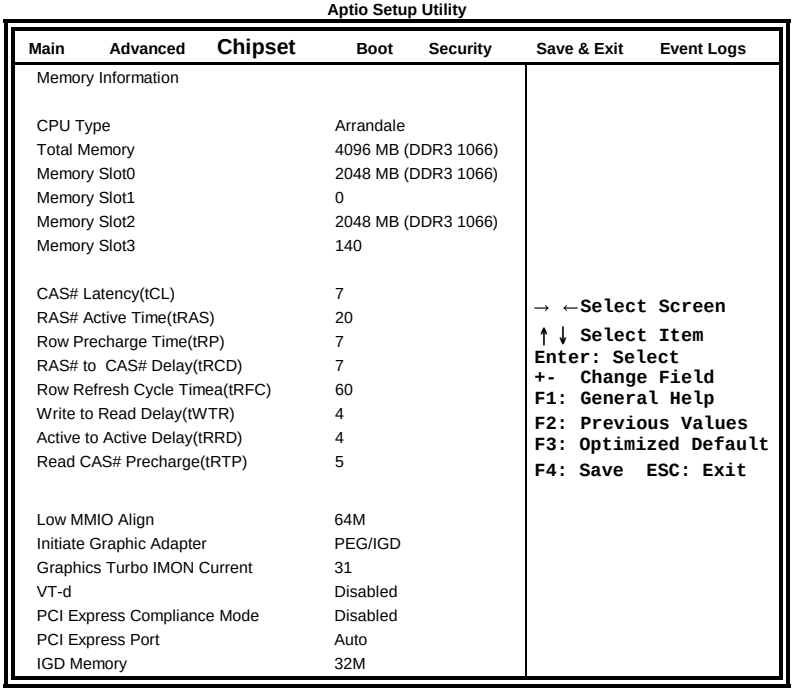
This item shows the South Bridge Parameters.

ME Subsystem

This item shows the ME Subsystem Parameters.

North Bridge

This section allows you to configure the North Bridge Chipset.



Low MMIO Align

Low MMIO resources align at 64MB/1024MB.

Initiate Graphic Adapter

Select which graphics controller to use as the primary boot device.
Options are IGD, PCI/IGD, PCI/PEG, PEG/IGD, PEG/PCI and SG.

Graphics Turbo IMON Current

Graphics turbo IMON current values supported (14-31).

VT-d

VT-d Enable/Disable.

PCI Express Compliance Mode

PCI Express Compliance Mode Enable/Disable.

PCI Express Port
Options are Disabled, Enabled and Auto.

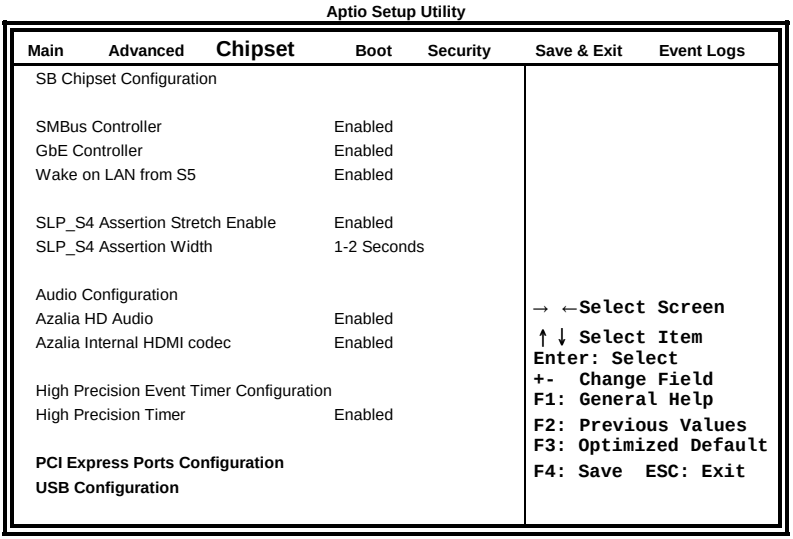
IGD Memory
IGD Share Memory Size. Options are Disable, 32M, 64M and 128M.

PAVP Mode
Select PAVP Mode used by Internal Graphics Device. Options are Disabled and Enabled.

PEG Force Gen1
PCI Express Port Force Gen1. Options are Disabled and

SB Chipset Configuration

This section allows you to configure the South Bridge Chipset.



SMBus Controller

SMBus Controller help.

GbE Controller

This is constantly enabled.

Wake on LAN from S5

Wake on LAN from S5 help.

SLP_S4 Assertion Stretch Enable

Select a minimum assertion width of the SLP_S4# signal.

Audio Configuration

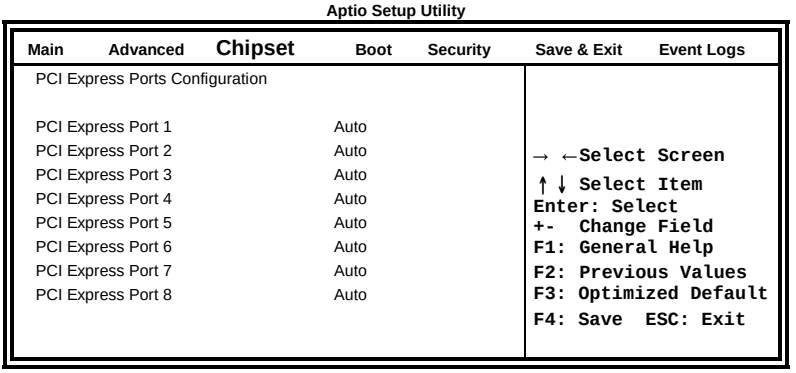
The Audio Configuration settings Enable/Disable the Azalia HD Audio and the Azalia internal HDMI codec.

High Precision Event Timer Configuration

Enable/or Disable the High Precision Event Timer.

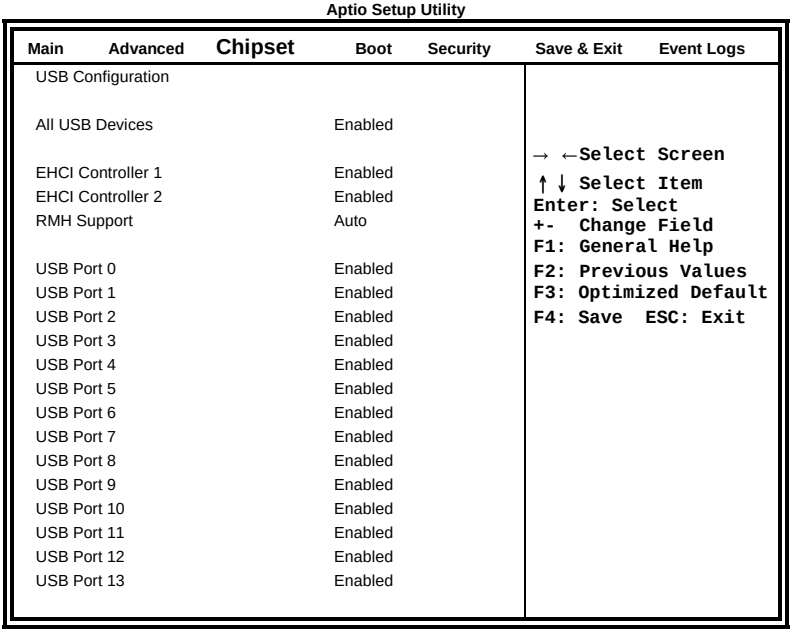
PCI Express Ports Configuration

Enable or Disable the PCI Express Ports in the Chipset.



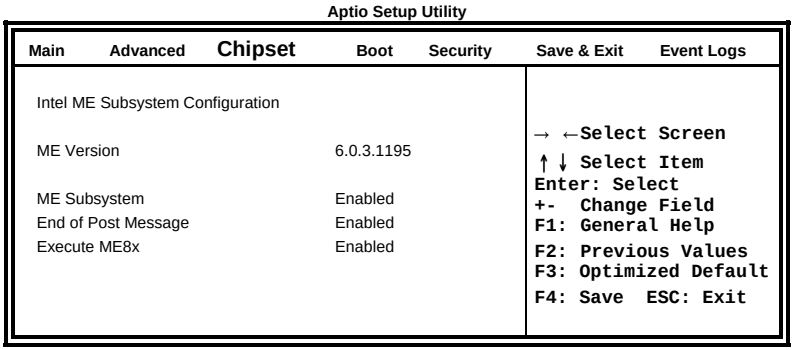
USB Configuration

Enable/Disable All USB Devices, USB 2.0 (EHCI) Support and RMH Support. The setting of AUTO on RMH Support Enable RMH support on Ibex Peak B0 Stepping.



Intel ME Subsystem

This section allows you to configure the PCI settings.



ME Version

Launches (Enabled/Disabled) the boot option for legacy network devices.

ME Subsystem

Launches (Enabled/Disabled) the boot option for legacy network devices.

End of Post Message

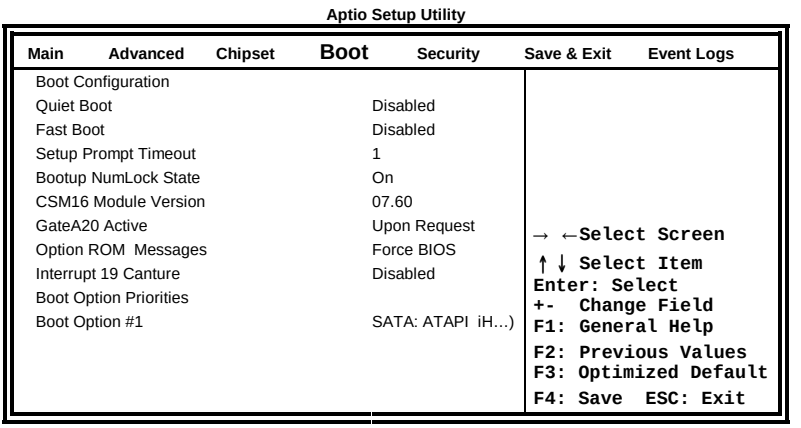
Launches (Enabled/Disabled) the boot option for legacy network devices.

Execute ME8x

Launches (Enabled/Disabled) the boot option for legacy network devices.

Boot Settings

This section allows you to configure the boot settings according to your preference.



Quiet Boot

Enables/Disables Quiet Boot option.

Fast Boot

Enables/Disables boot with initialization of a minimal set of devices required to launch active boot option. Has no effect for BBS boot options.

Setup Prompt Timeout

Number of seconds to wait for setup activation key.
65535(0xFFFF) means indefinite waiting.

Bootup NumLock State

Select the keyboard NumLock state.

GateA20 Active

UPON REQUEST – GA20 can be disabled using BIOS services.
ALWAYS – do not allow disabling GA20; this option is useful when any RT code is executed above 1MB.

Option ROM Messages

Set display mode for Option ROM. Options are Force BIOS and Keep Current.

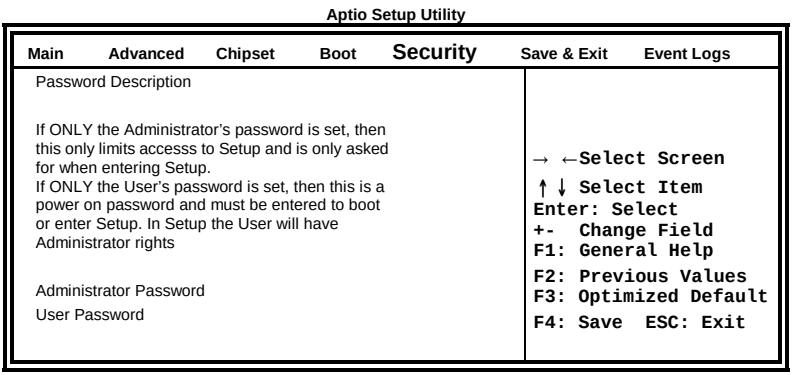
Interrupt 19 Canture

Enable: Allows Option ROMs to trap Int 19.

Boot Option Priorities
Sets the system boot order.

Hard Drive BBS Priorities
Set the order of the legacy devices in this group.

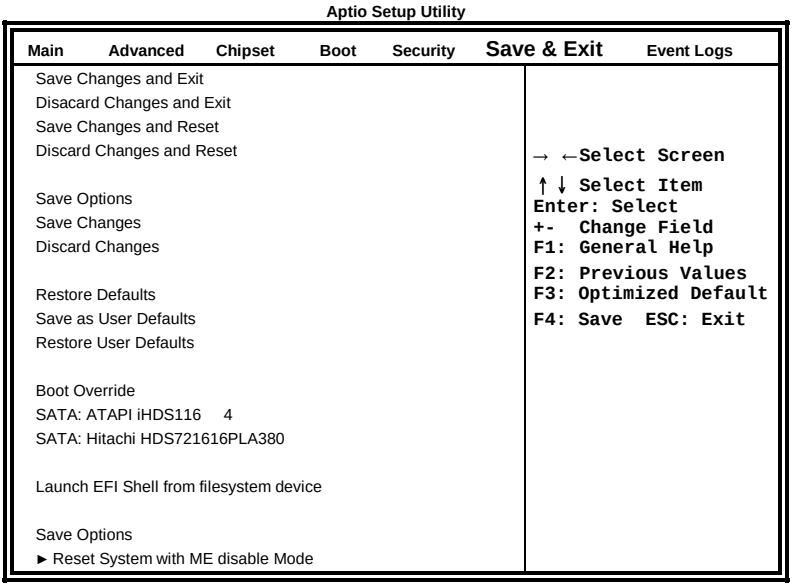
Security Settings
This section allows you to configure and improve your system and allows you to set up some system features according to your preference.



Administrator Password
Set Setup Administrator Password.

User Password
Set User Password.

Save & Exit Settings



Save Changes and Exit
Exit system setup after saving the changes.

Disacard Changes and Exit
Exit system setup without saving any changes.

Save Changes and Reset
Reset the system after saving the changes.

Discard Changes and Reset
Reset system setup without saving any changes.

Save Changes
Save Changes done so far to any of the setup options.

Discard Changes
Discard Changes done so far to any of the setup options.

Restore Defaults
Restore/Load Defaults values for all the setup options.

Save as User Defaults
Save the changes done so far as User Defaults.

Restore User Defaults
Restore the User Defaults to all the setup options.

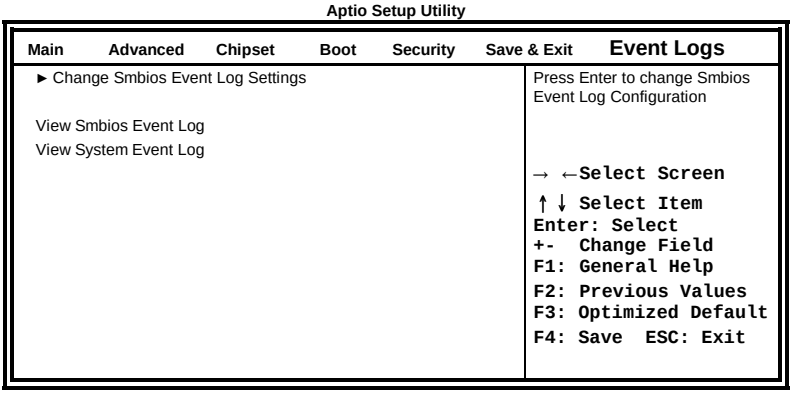
Boot Override
Pressing ENTER causes the system to enter the OS.

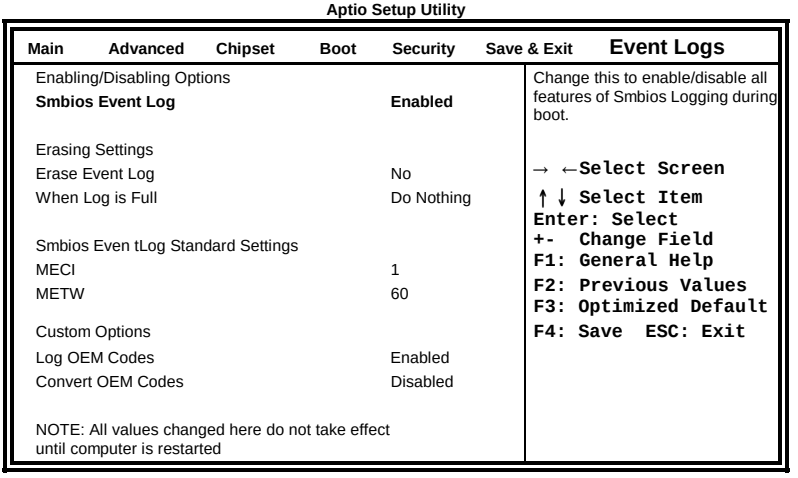
Launch EFI Shell from filesystem device
Attempts to Launch EFI Shell application (Shellx64.efi) from one of the available filesystem devices.

Reset System with ME disable Mode
ME will run into the temporary disable mode.

Event Logs

This section allows you to configure the Smbios Event Log. according to your preference.





Drivers Installation

This section describes the installation procedures for software and drivers under Windows operating systems. The software and drivers are included with the motherboard. If you find the items missing, please contact the vendor where you made the purchase. The contents of this section include the following:

Intel Chipset Software Installation Utility

The Intel Chipset Drivers should be installed first before the software drivers to enable Plug & Play INF support for Intel chipset components. Follow the instructions below to complete the installation.

1. Insert the CD that comes with the board. Click ***Intel*** and then ***Intel(R) QM57 Chipset Drivers***.

2. Click ***Intel(R) Chipset Software Installation Utility.***

3. When the Welcome screen to the Intel® Chipset Device Software appears, click ***Next*** to continue.

4. Click ***Yes*** to accept the software license agreement and proceed with the installation process.

5. On the Readme File Information screen, click ***Next*** to continue the installation.

6. The Setup process is now complete. Click ***Finish*** to restart the computer and for changes to take effect.

VGA Drivers Installation

NOTE: Before installing the *Intel(R) QM57 Chipset Family Graphics Driver,* the Microsoft .NET Framework 3.5 SPI should be first installed.

To install the VGA drivers, follow the steps below.
1. Insert the CD that comes with the board. Click ***Intel*** and then ***Intel(R) QM57 Chipset Drivers***.

2. Click ***Intel(R) QM57 Chipset Family Graphics Driver.***

3. When the Welcome screen appears, click ***Next*** to continue.

4. Click ***Yes*** to to agree with the license agreement and continue the installation.

5. On the Readme File Information screen, click ***Next*** to continue the installation of the Intel® Graphics Media Accelerator Driver.

6. On Setup Progress screen, click ***Next*** to continue.

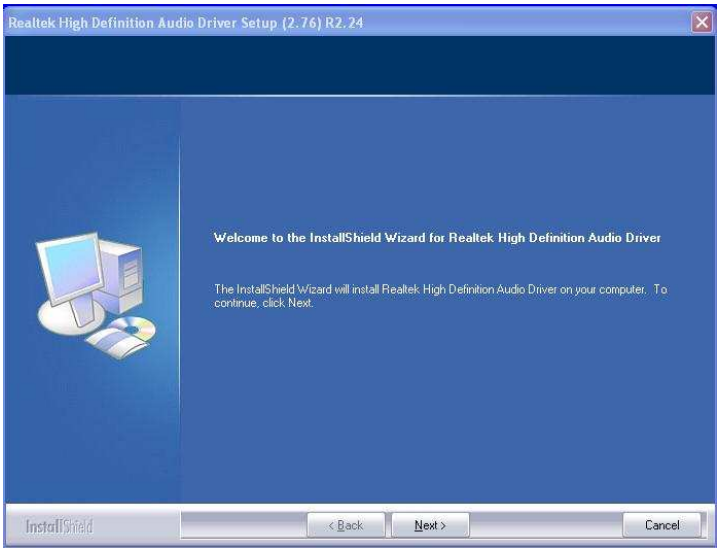
7. Setup complete. Click ***Finish*** to restart the computer and for changes to take effect.

Realtek HD Audio Driver Installation

Follow the steps below to install the Realtek HD Audio Drivers.
1. Insert the CD that comes with the board. Click ***Intel*** and then ***Intel(R) QM57 Chipset Drivers***.

2. Click ***Realtek High Definition Audio Driver.***

3. On the Welcome to the InstallShield Wizard screen, click ***Next***.



3. InstallShield Wizard is complete. Click ***Finish*** to restart the computer.

LAN Drivers Installation

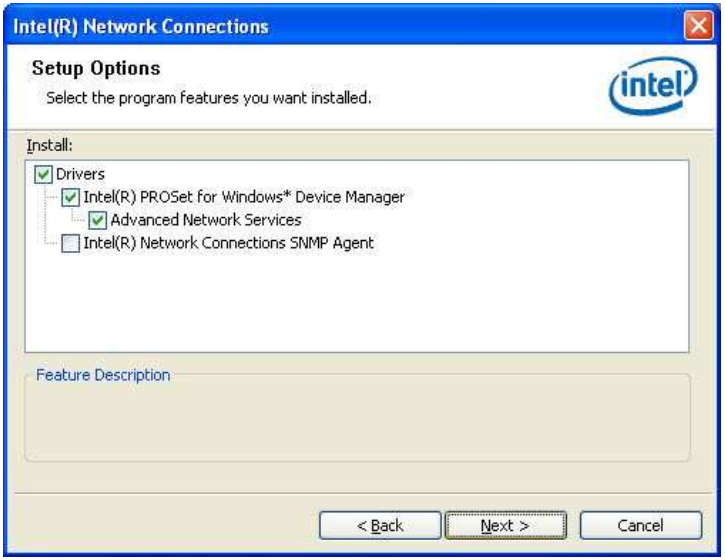
Follow the steps below to install the Intel LAN drivers.

1. Insert the CD that comes with the board. Click ***Intel*** and then ***Intel(R) QM57 Chipset Drivers***.

2. Click ***Intel(R) PRO LAN Network Driver.***

3. When the Welcome screen appears, click ***Next***. On the next screen, click ***Yes*** to to agree with the license agreement.

4. Click the checkbox for **Drivers** in the Setup Options screen to select it and click **Next** to continue.



5. The wizard is ready to begin installation. Click ***Install*** to begin the installation.

6. When InstallShield Wizard is complete, click ***Finish***.

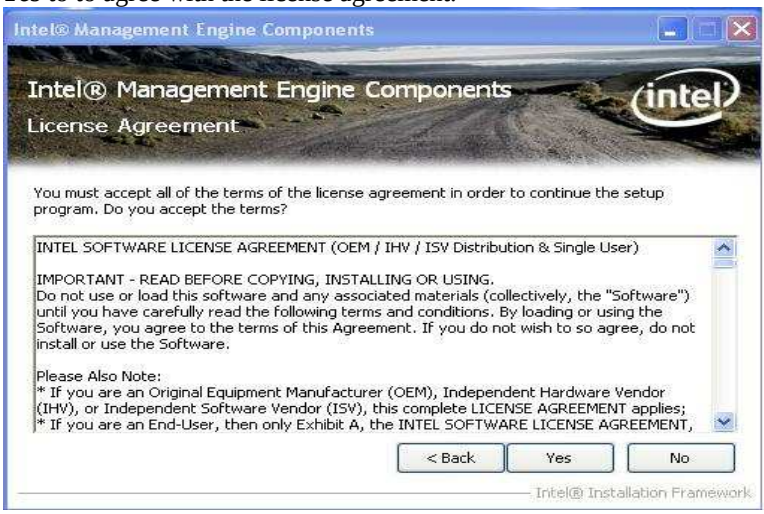
Intel® Management Engine Interface

NOTE: Before installing the *Intel(R) AMT 6.0 Drivers,* the Microsoft .NET Framework 3.5 SPI should be first installed.

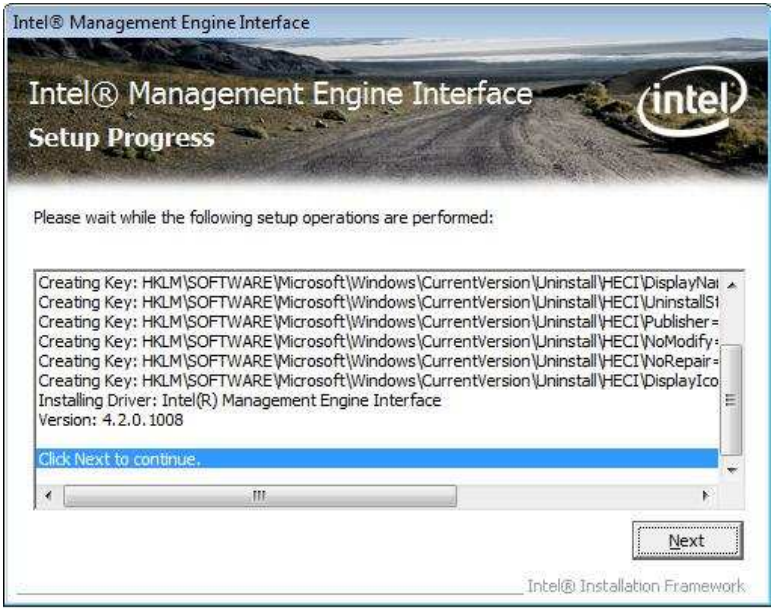
Follow the steps below to install the Intel Management Engine.

1. Insert the drivers disc that comes with the motherboard. Click ***Intel*** and then ***Intel(R) AMT 6.0 Drivers***.

2. When the Welcome screen to the InstallShield Wizard for Intel® Management Engine Components, click ***Next***. On the next screen, click ***Yes*** to to agree with the license agreement.



2. When the Setup Progress screen appears, click ***Next***. Then, click ***Finish*** when the setup progress has been successfully installed.




Intel® Management Engine Interface
Intel® Management Engine Interface
Setup Is Complete
intel
The setup program successfully installed the Intel® Management Engine Interface onto this computer. Click Finish to complete the setup process.
Finish
Intel® Installation Framework

Appendix

A. I/O Port Address Map

Each peripheral device in the system is assigned a set of I/O port addresses which also becomes the identity of the device. The following table lists the I/O port addresses used.

Address	Device Description
000h - 01Fh	DMA Controller #1
020h - 03Fh	Interrupt Controller #1
040h - 05Fh	Timer
060h - 06Fh	Keyboard Controller
070h - 07Fh	Real Time Clock, NMI
080h - 09Fh	DMA Page Register
0A0h - 0BFh	Interrupt Controller #2
0C0h - 0DFh	DMA Controller #2
0F0h	Clear Math Coprocessor Busy Signal
0F1h	Reset Math Coprocessor
1F0h - 1F7h	IDE Interface
278h - 27Fh	Parallel Port #2(LPT2)
2E8h – 2EFh	Serial Port #4(COM4)
2F8h - 2FFh	Serial Port #2(COM2)
2B0h- 2DFh	Graphics adapter Controller
360h - 36Fh	Network Ports
3B0h - 3BFh	Monochrome & Printer adapter
3C0h - 3CFh	EGA adapter
3D0h - 3DFh	CGA adapter
3E8h – 3EFh	Serial Port #3(COM3)
3F8h - 3FFh	Serial Port #1(COM1)

B. Interrupt Request Lines (IRQ)

Peripheral devices use interrupt request lines to notify CPU for the service required. The following table shows the IRQ used by the devices on board.

Level	Function
IRQ0	System Timer Output
IRQ1	Keyboard
IRQ2	Interrupt Cascade
IRQ3	Serial Port #2
IRQ4	Serial Port #1
IRQ5	Reserved
IRQ6	Reserved
IRQ7	Reserved
IRQ8	Real Time Clock
IRQ9	Reserved
IRQ10	Serial Port #3
IRQ11	Serial Port #4
IRQ12	PS/2 Mouse
IRQ13	80287
IRQ14	Primary IDE
IRQ15	Secondary IDE

C. Watchdog Timer Configuration

The WDT is used to generate a variety of output signals after a user programmable count. The WDT is suitable for use in the prevention of system lock-up, such as when software becomes trapped in a deadlock. Under these sorts of circumstances, the timer will count to zero and the selected outputs will be driven. Under normal circumstance, the user will restart the WDT at regular intervals before the timer counts to zero.

SAMPLE CODE:

```
//---------------------------------------------------------------------------
//
// THIS CODE AND INFORMATION IS PROVIDED "AS IS" WITHOUT WARRANTY OF ANY
// KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE
// IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A PARTICULAR
// PURPOSE.
//
//---------------------------------------------------------------------------
#include <dos.h>
#include <conio.h>
#include <stdio.h>
#include <stdlib.h>
#include "F81865.H"
//---------------------------------------------------------------------------
int main (int argc, char *argv[]);
void EnableWDT(int);
void DisableWDT(void);
//---------------------------------------------------------------------------
int main (int argc, char *argv[])
{
        unsigned char bBuf;
        unsigned char bTime;
        char **endptr;

        char SIO;

        printf("Fintek 81865 watch dog program\n");

        SIO = Init_F81865();
        if (SIO == 0)
        {
                printf("Can not detect Fintek 81865, program abort.\n");
                return(1);
        }//if (SIO == 0)

        if (argc != 2)
        {
                printf(" Parameter incorrect!!\n");
                return (1);
        }

        bTime = strtol (argv[1], endptr, 10);
        printf("System will reset after %d seconds\n", bTime);

        if (bTime)
        {       EnableWDT(bTime);  }
        else
        {       DisableWDT();          }
```

```
        return 0;
}
//---------------------------------------------------------------------------
void EnableWDT(int interval)
{
        unsigned char bBuf;

        bBuf = Get_F81865_Reg(0x2B);
        bBuf &= (~0x20);
        Set_F81865_Reg(0x2B, bBuf);                     //Enable WDTO

        Set_F81865_LD(0x07);                            //switch to logic device 7
        Set_F81865_Reg(0x30, 0x01);                     //enable timer

        bBuf = Get_F81865_Reg(0xF5);
        bBuf &= (~0x0F);
        bBuf |= 0x52;
        Set_F81865_Reg(0xF5, bBuf);                     //count mode is second

        Set_F81865_Reg(0xF6, interval);                 //set timer

        bBuf = Get_F81865_Reg(0xFA);
        bBuf |= 0x01;
        Set_F81865_Reg(0xFA, bBuf);                     //enable WDTO output

        bBuf = Get_F81865_Reg(0xF5);
        bBuf |= 0x20;
        Set_F81865_Reg(0xF5, bBuf);                     //start counting
}
//---------------------------------------------------------------------------
void DisableWDT(void)
{
        unsigned char bBuf;

        Set_F81865_LD(0x07);                            //switch to logic device 7

        bBuf = Get_F81865_Reg(0xFA);
        bBuf &= ~0x01;
        Set_F81865_Reg(0xFA, bBuf);                     //disable WDTO output

        bBuf = Get_F81865_Reg(0xF5);
        bBuf &= ~0x20;
        bBuf |= 0x40;
        Set_F81865_Reg(0xF5, bBuf);                     //disable WDT
}
//---------------------------------------------------------------------------
```

```
//---------------------------------------------------------------------------
//
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// KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE
// IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A PARTICULAR
// PURPOSE.
//
//---------------------------------------------------------------------------
#include "F81865.H"
#include <dos.h>
//---------------------------------------------------------------------------
unsigned int F81865_BASE;
void Unlock_F81865 (void);
void Lock_F81865 (void);
//---------------------------------------------------------------------------
unsigned int Init_F81865(void)
{
	unsigned int result;
	unsigned char ucDid;

	F81865_BASE = 0x4E;
	result = F81865_BASE;

	ucDid = Get_F81865_Reg(0x20);
	if (ucDid == 0x07)                                  //Fintek 81865
	{	goto Init_Finish;	}

	F81865_BASE = 0x2E;
	result = F81865_BASE;

	ucDid = Get_F81865_Reg(0x20);
	if (ucDid == 0x07)                                  //Fintek 81865
	{	goto Init_Finish;	}

	F81865_BASE = 0x00;
	result = F81865_BASE;

Init_Finish:
	return (result);
}
//---------------------------------------------------------------------------
void Unlock_F81865 (void)
{
	outportb(F81865_INDEX_PORT, F81865_UNLOCK);
	outportb(F81865_INDEX_PORT, F81865_UNLOCK);
}
//---------------------------------------------------------------------------
void Lock_F81865 (void)
{
	outportb(F81865_INDEX_PORT, F81865_LOCK);
}
//---------------------------------------------------------------------------
void Set_F81865_LD( unsigned char LD)
{
	Unlock_F81865();
	outportb(F81865_INDEX_PORT, F81865_REG_LD);
	outportb(F81865_DATA_PORT, LD);
	Lock_F81865();
}
//---------------------------------------------------------------------------
void Set_F81865_Reg( unsigned char REG, unsigned char DATA)
{
	Unlock_F81865();
	outportb(F81865_INDEX_PORT, REG);
	outportb(F81865_DATA_PORT, DATA);
	Lock_F81865();
}
//---------------------------------------------------------------------------
```

```
unsigned char Get_F81865_Reg(unsigned char REG)
{
        unsigned char Result;
        Unlock_F81865();
        outportb(F81865_INDEX_PORT, REG);
        Result = inportb(F81865_DATA_PORT);
        Lock_F81865();
        return Result;
}
//-----------------------------------------------------------------------------
```

```
//-----------------------------------------------------------------------------
//
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// KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE
// IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A PARTICULAR
// PURPOSE.
//
//-----------------------------------------------------------------------------
#ifndef __F81865_H
#define __F81865_H                     1
//-----------------------------------------------------------------------------
#defineF81865_INDEX_PORT        (F81865_BASE)
#defineF81865_DATA_PORT         (F81865_BASE+1)
//-----------------------------------------------------------------------------
#defineF81865_REG_LD            0x07
//-----------------------------------------------------------------------------
#define F81865_UNLOCK           0x87
#defineF81865_LOCK                      0xAA
//-----------------------------------------------------------------------------
unsigned int Init_F81865(void);
void Set_F81865_LD( unsigned char);
void Set_F81865_Reg( unsigned char, unsigned char);
unsigned char Get_F81865_Reg( unsigned char);
//-----------------------------------------------------------------------------
#endif  //__F81865_H
```